

COMPAL CONFIDENTIAL

MODEL NAME : VALA0

PCB NO : LA-9411P

GPIO P/N: 2012.12.20 Rev 3.0C

BOM P/N :

4319L231L01 SMT MB A9411 VALA0 DSC TPM R1

4319L231L02 SMT MB A9411 VALA0 DSC DTP R1

4319L231L03 SMT MB A9411 VALA0 DSC TPM WO EXP R1

4319L231L04 SMT MB A9411 VALA0 DSC DTP WO EXP R1

4319L231L05 SMT MB A9411 VALA0 DSC TPM R1

4319L231L06 SMT MB A9411 VALA0 DSC DTP R1

4319L231L07 SMT MB A9411 VALA0 DSC TPM WO EXP R1

4319L231L08 SMT MB A9411 VALA0 DSC DTP WO EXP R1

SALADO 15 HSW

HASWELL + LYNX POINT

2013_04_10

REV : 1.0 (A00)

@ : Nopop Component

CONN@ : Connector Component

www.aitech1.ru

15MDC@ : MDC

L01/L02/L5/L6

V

L03/L04/L7/L8

V

15G@ : Only for 15 Discrete

V

V

PXDP@ : PCH XDP

EMC@ : EMI/ESD/RF

V

V

EXP@ : Express Card


V

V

CXDP@ : CPU XDP

MB PCB	
Part Number	Description
DAA00005Q00	PCB 0LH LA-9411P REV0 M/B DSC

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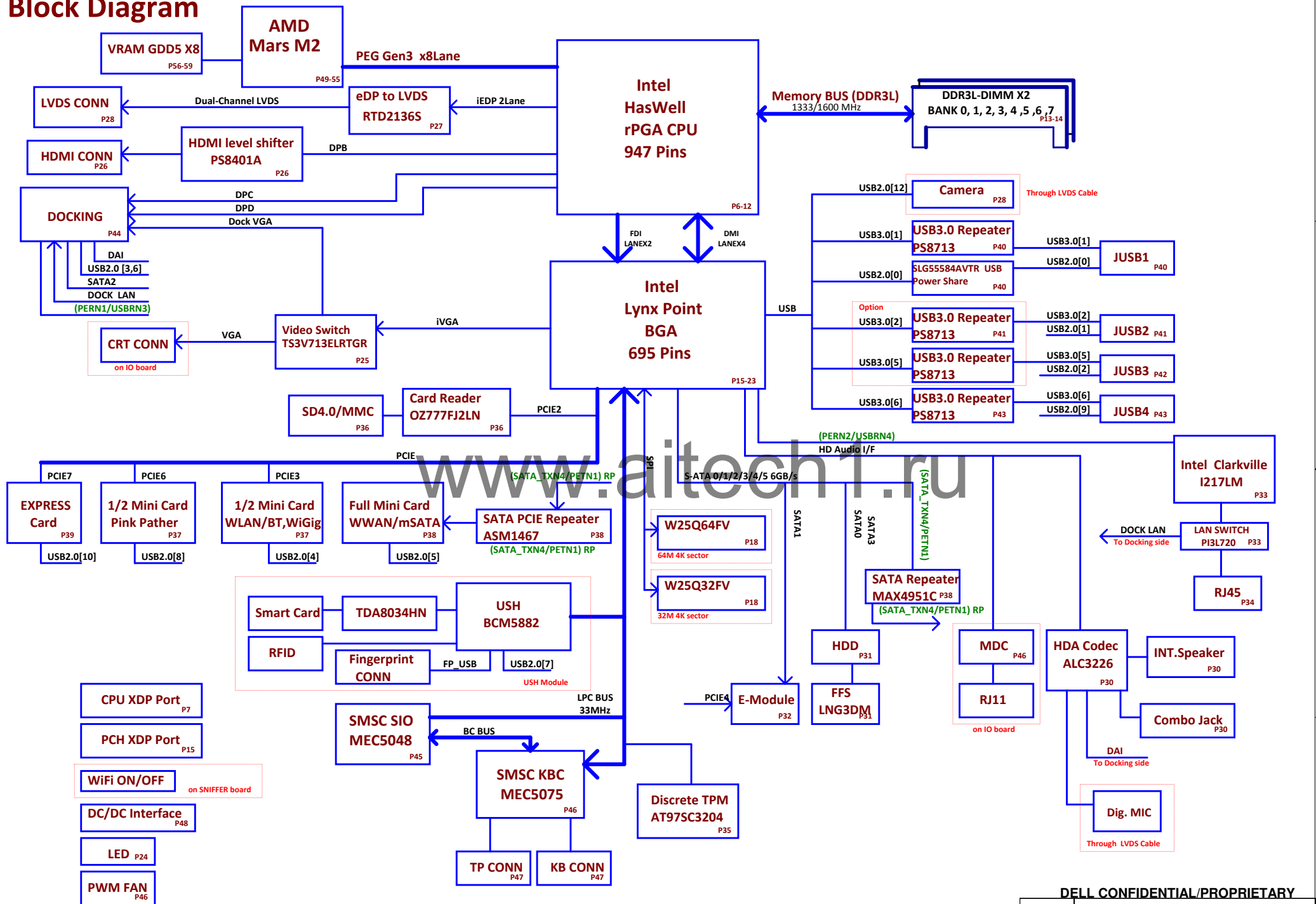
Cover Page

LA-9411P

Date: Wednesday, April 10, 2013 Sheet 1 of 77

Title	Document Number	Rev
	LA-9411P	1.0

Block Diagram



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POWER STATES

State \ Signal	SLP S3#	SLP S4#	SLP S5#	SLP A#	ALWAYS PLANE	M PLANE	SUS PLANE	RUN PLANE	CLOCKS
S0 (Full ON) / M0	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON	ON
S3 (Suspend to RAM) / M3	LOW	HIGH	HIGH	HIGH	ON	ON	ON	OFF	OFF
S4 (Suspend to DISK) / M3	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF	OFF
S5 (SOFT OFF) / M3	LOW	LOW	LOW	HIGH	ON	ON	OFF	OFF	OFF
S3 (Suspend to RAM) / M-OFF	LOW	HIGH	HIGH	LOW	ON	OFF	ON	OFF	OFF
S4 (Suspend to DISK) / M-OFF	LOW	LOW	HIGH	LOW	ON	OFF	OFF	OFF	OFF
S5 (SOFT OFF) / M-OFF	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF	OFF

PM TABLE

State \ power plane	+PWR_SRC +PWR_SRC_S +5V_ALW +3.3V_ALW +3.3V_ALW_PCH +3.3V_RTC_LDO	+3.3V_SUS +1.35V_MEM	+5V_RUN +3.3V_RUN +1.5V_RUN +0.675V_DDR_VTT +VCC_CORE +1.05V_RUN +GPU_CORE +1.35V_MEM_GFX +1.8V_RUN_GFX +VGA_PCIE +3.3V_RUN_GFX +VDDCI	+3.3V_M +1.05V_M	+3.3V_M +1.05V_M (M-OFF)
S0	ON	ON	ON	ON	ON
S3	ON	ON	OFF	ON	OFF
S5 S4/AC	ON	OFF	OFF	ON	OFF
S5 S4/AC don't exist	OFF	OFF	OFF	OFF	OFF

PCH	USB 2.0 PORT#	USB 3.0 PORT#	DESTINATION
	0	1	Right Side Top (JUSB1)
	1	2	Right Side Middle (JUSB2)
	2	5	Right Side bottom (JUSB3)
	3	3 (PERN1/USBRN3)	DOCKING (JDOCK1)
	4		WLAN (JMINI2)
	5		WWAN (JMINI1)
	6		DOCKING (JDOCK1)
	7		USH (JUSH1)
	8		Pink Pather (JMINI3)
	9	6	Left Side (JUSB4)
	10		Express card (JEXP1)
	11		None
	12		CAMERA (JCAM1)
	13		None

PCI EXPRESS	DESTINATION
Lane 1 (SATA_TXN4/PETN1)	WWAN (JMINI1) <small>SATA by default</small>
Lane 2 (SATA_RXN5/PERN2)	None
Lane 2 (PERN2/USBRN4)	10/100/1G LOM
Lane 3	WLAN (JMINI2)
Lane 4	E3 Module Bay (JSATA2)
Lane 5	None
Lane 6	Pink Pather (JMINI3)
Lane 7	Express card (JEXP1)
Lane 8	MMI

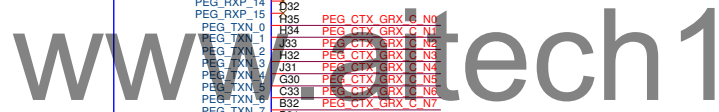
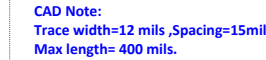
SATA	DESTINATION
SATA 0	HDD (JSATA1)
SATA 1	ODD (JSATA2)
SATA 2	Dock (JDOCK1)
SATA 3	NA
SATA 4 (SATA_TXN4/PETN1)	WWAN (JMINI1) <small>SATA by default</small>

DISPLAY Ports On CPU	Connetion
DDIB	MB HDMI (JHDMI1)
DDIC	Dock DP port 1
DDID	Dock DP port 2

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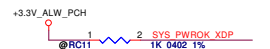
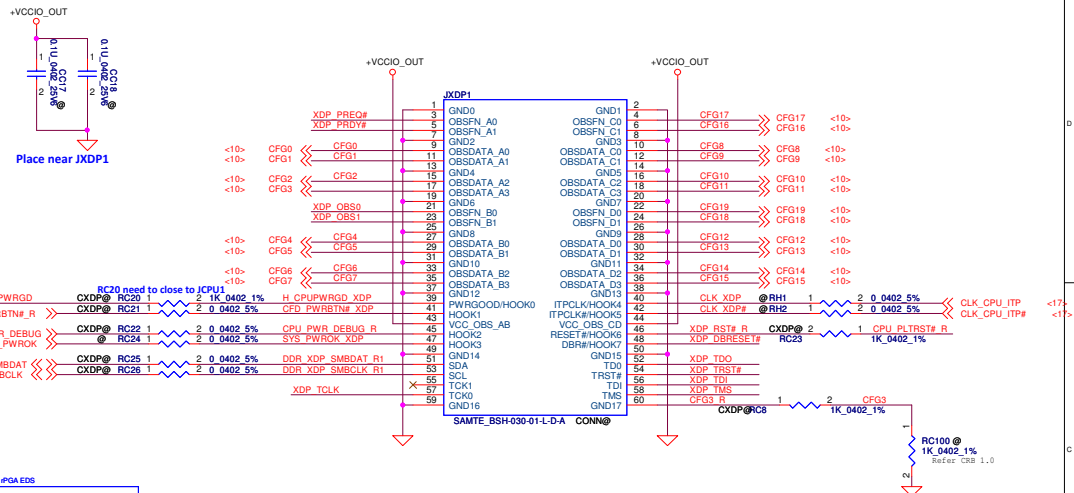
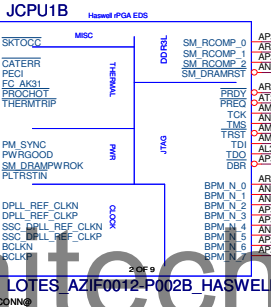
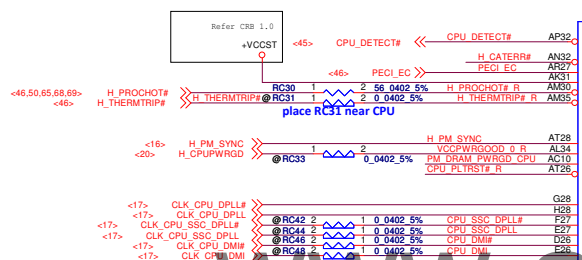
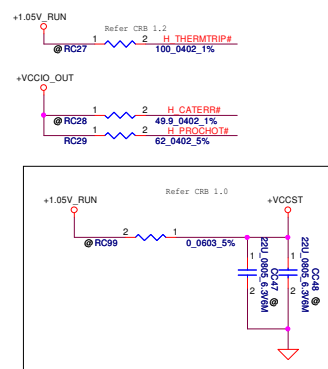


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Index and Configuration			
File	Document Number	Rev	
	LA-9411P	1.0	
Date:	Wednesday, April 10, 2013	Sheet	3 of 77



Title			
CPU (1/7)			
Size	Document Number		Rev
	LA-9411P		1.0
Date:	Wednesday, April 10, 2013		Sheet 6 of 77

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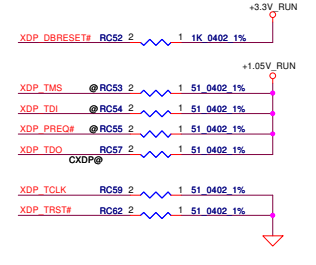
Buffered reset to CPU

CAD Note:
PLACE PULL-UP RESISTOR WITHIN 2 INCH OF THE CPU

CAD Note:
Avoid stub in the PWRGD path while placing resistors RC33 & RC56

SM RCOMP0	RC58	1		2	100_0402	1%
SM RCOMP1	RC61	1		2	75_0402	1%
SM RCOMP2	RC63	1		2	100_0402	1%

CAD Note:
Trace width=12~15 mil, Spcing=20 mils
Max trace length= 500 mil



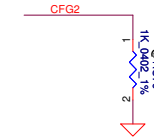
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CPU (2/7)

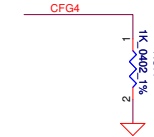
LA-9411P

Date: Wednesday, April 10, 2013 Sheet 7 of 77

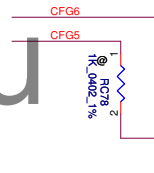
CFG STRAPS for CPU



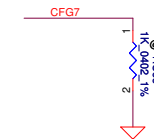
PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	1:(Default) Normal Operation; Lane # definition matches socket pin map definition 0:Lane Reversed



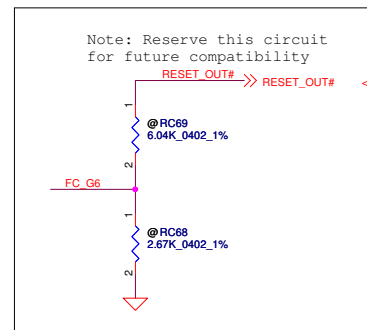
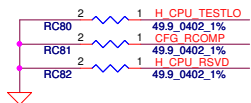
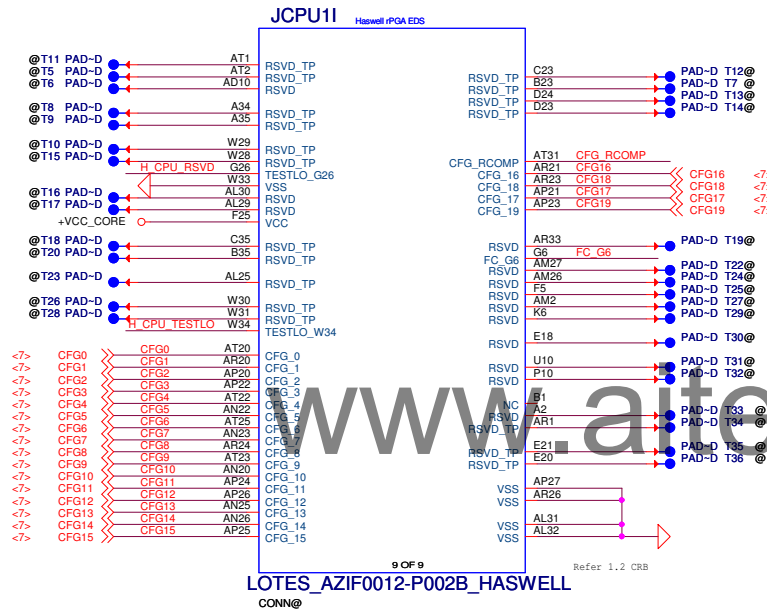
Display Port Presence Strap	
CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port



PCIe Port Bifurcation Straps	
CFG[6:5]	11: (Default) x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled



PEG DEFER TRAINING	
CFG7	1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training



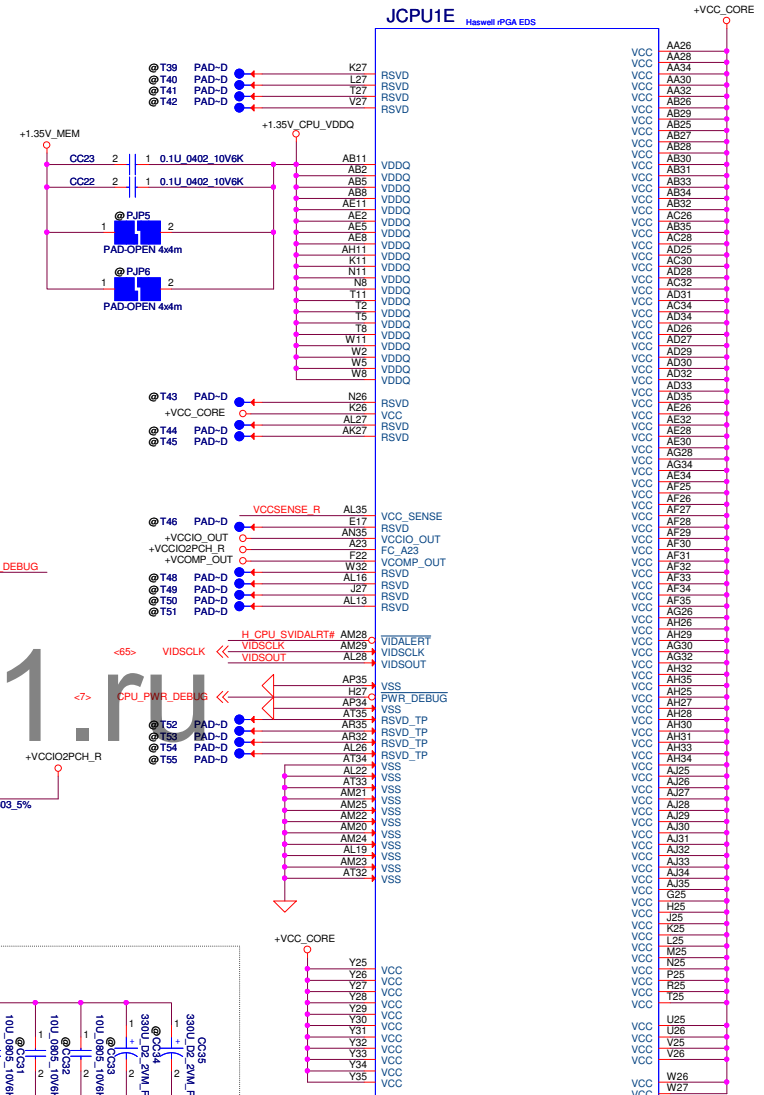
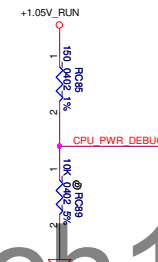
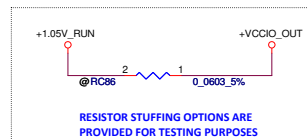
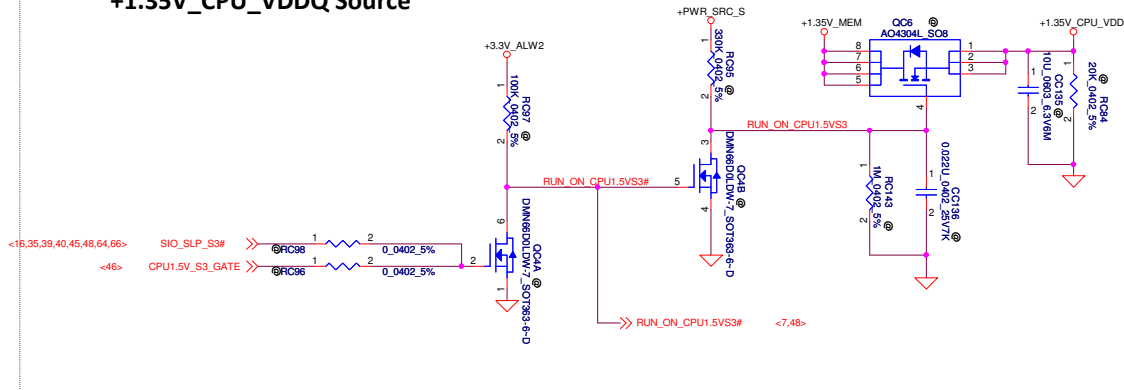
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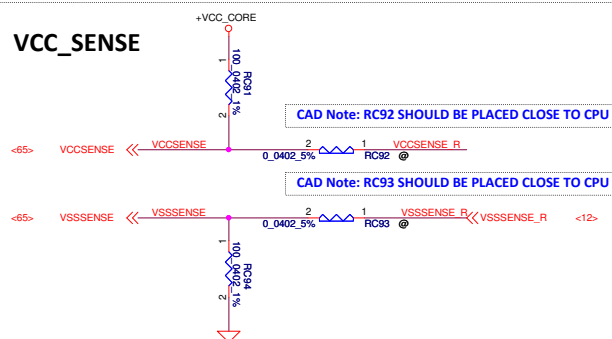
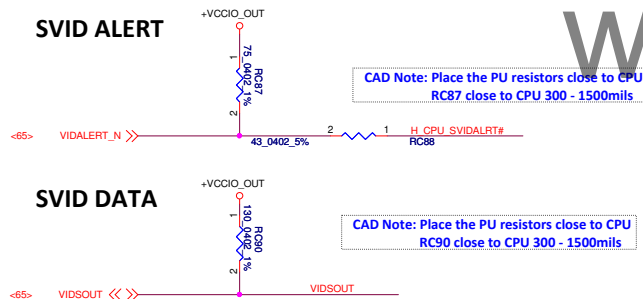
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Title CPU (5/7)			
Size	Document Number	Rev LA-9411P	
Date: Wednesday, April 10, 2013	Sheet 10	of 77	

16,35,39,40,45,48,64,66> SIO_SLP_S3# >> RC98 1 2 0_0402_5%

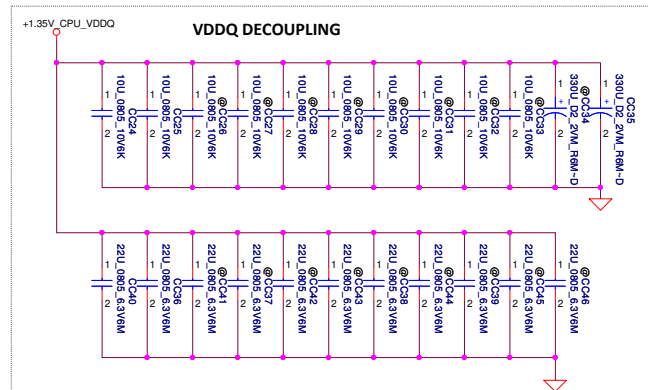
<46> CPU1.5V_S3_GATE >> RC96 1 2 0_0402_5%



SVID DATA



1 2U_08



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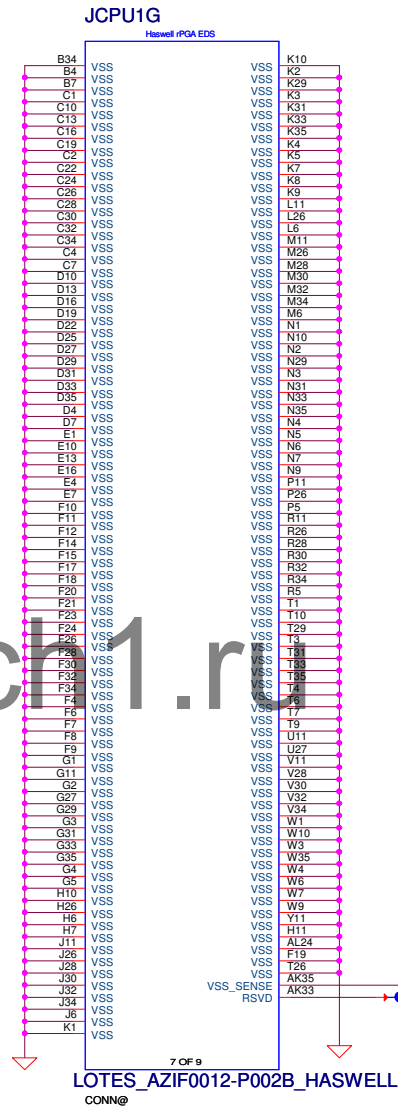
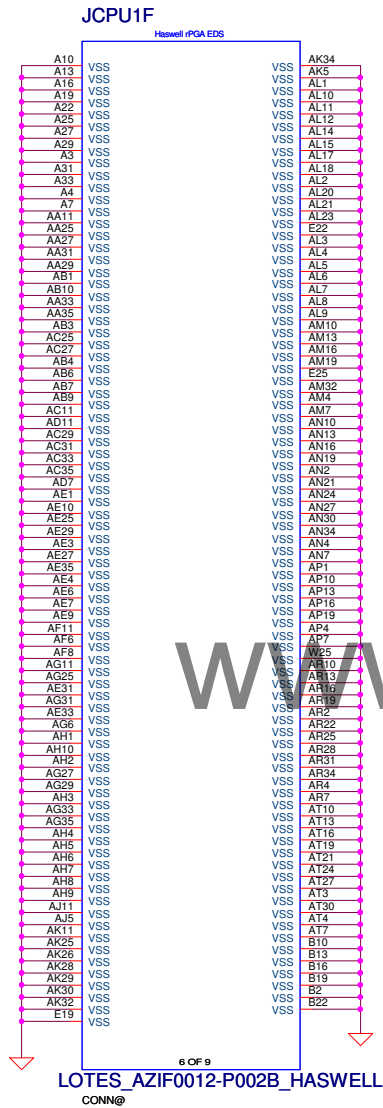
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CPU (6/7)

LA-9411P

LA-9411P

Date: Wednesday, April 10, 2013 Sheet 11 of 77

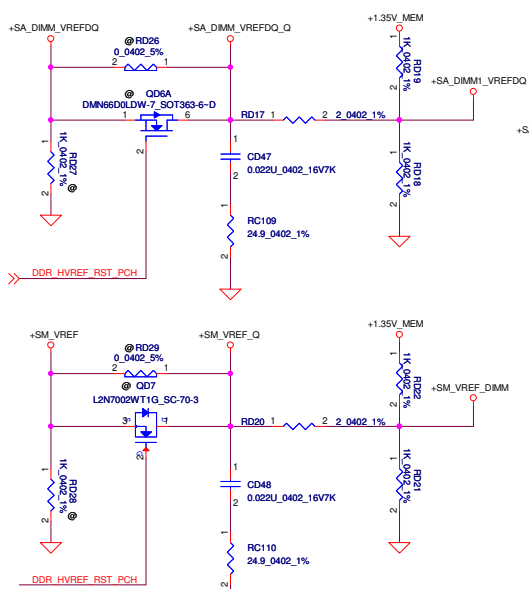


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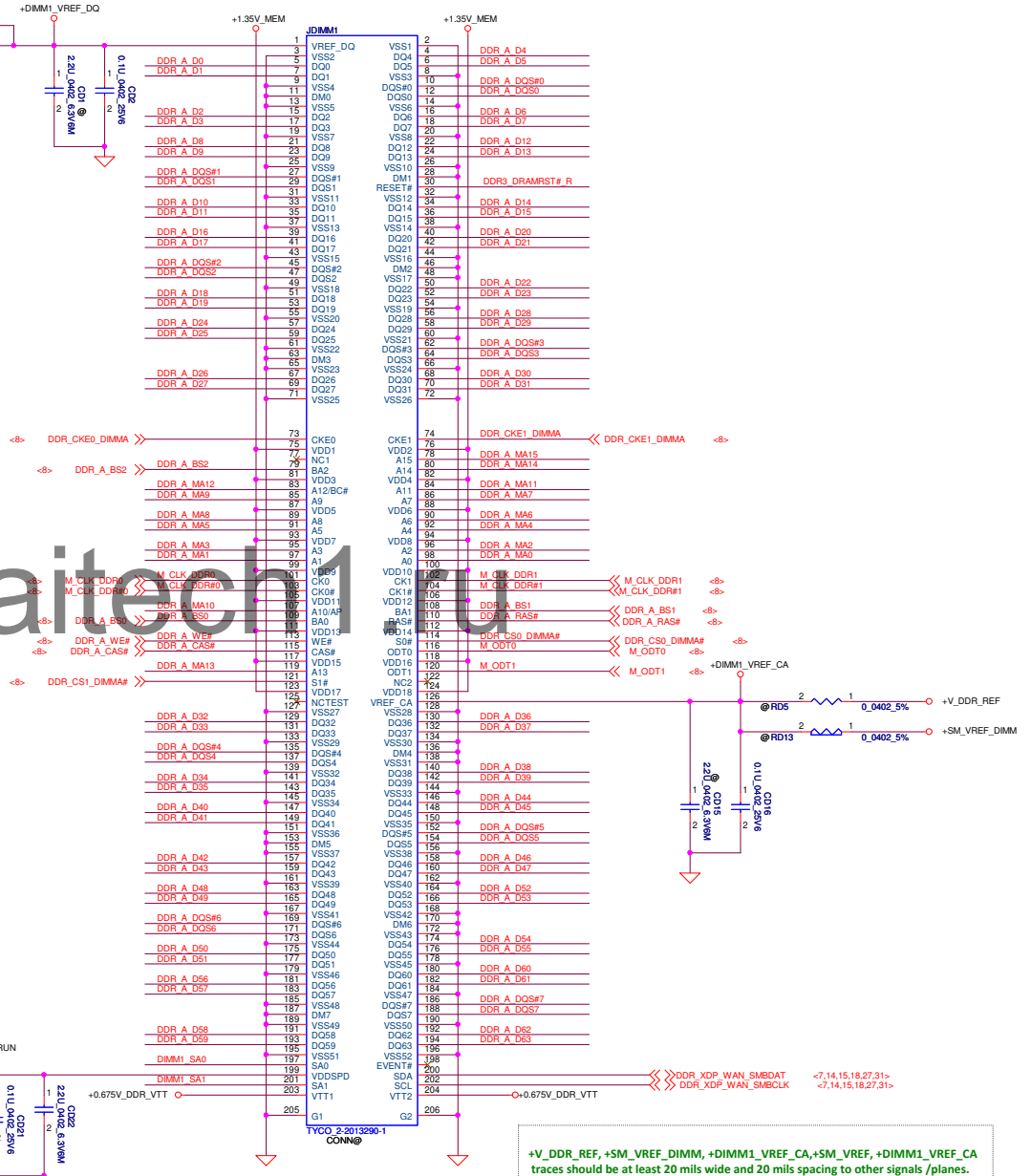


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Title			
CPU (7/7)			
Size	Document Number	Rev	
	LA-9411P	1.0	
Date:	Wednesday, April 10, 2013	Sheet	12 of 77



Populate RD1, De-Populate RD3 for Intel DDR3 VREFDQ multiple methods M1
Populate RD7, De-Populate RD1 for Intel DDR3 VREFDQ multiple methods M3

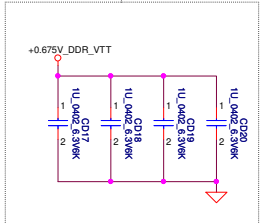
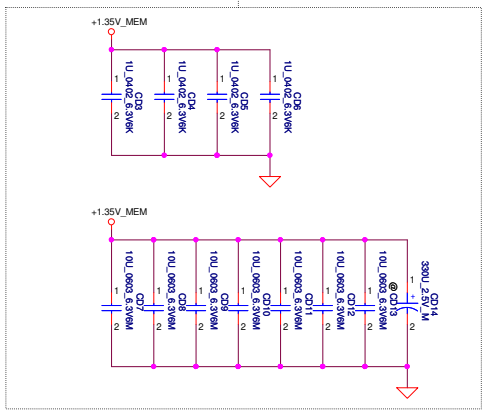
JDIMM1 H=5.2mm



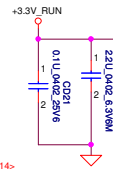
+V_DDR_REF, +SA_DIMM1_VREFDQ, +SA_DIMM_VREFDQ, +DIMM1_VREF_DQ traces should be at least 20 mils wide and 20 mils spacing to other signals /planes.

Layout Note:
Place near JDIMM1

Layout Note:
Place near JDIMM1,203,204



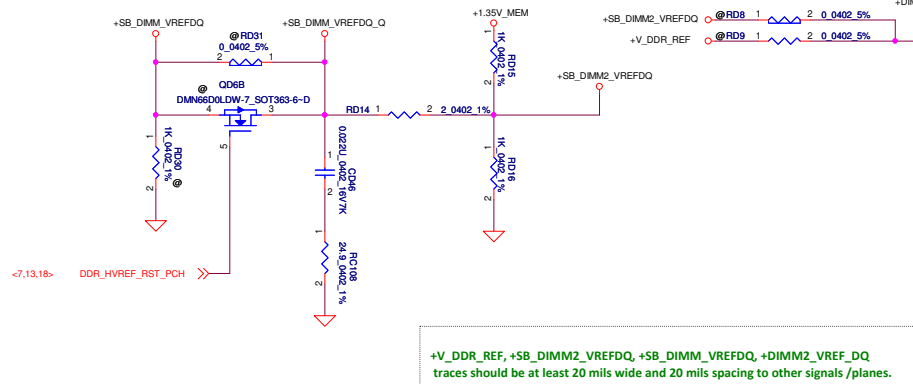
All VREF traces should have 10 mil trace width



+V_DDR_REF, +SM_VREF_DIMM, +DIMM1_VREF_CA, +SM_VREF, +DIMM1_VREF_CA traces should be at least 20 mils wide and 20 mils spacing to other signals /planes.

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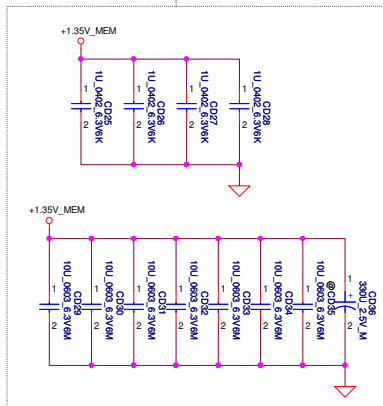
JDIMM2 H=9.2mm



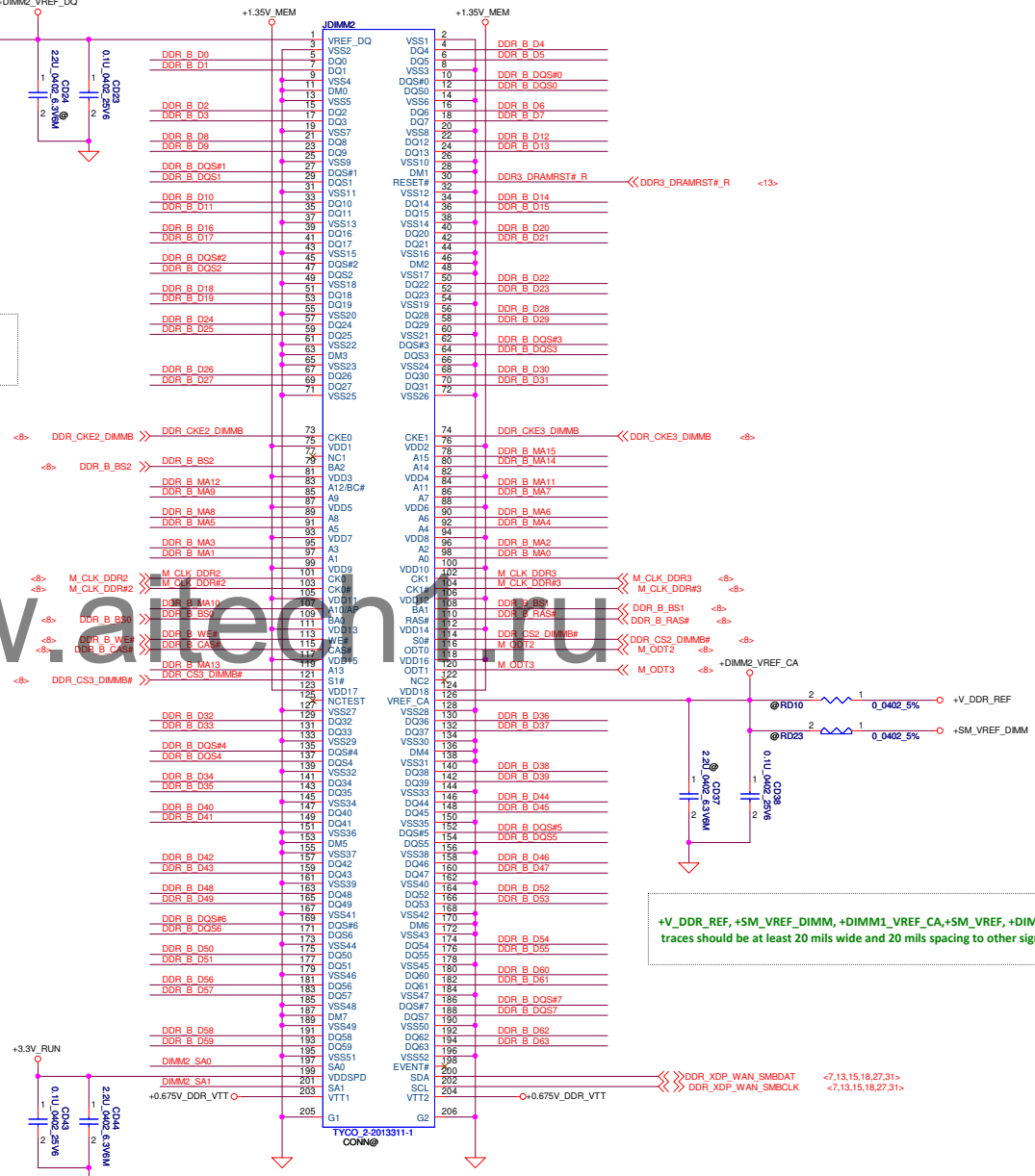
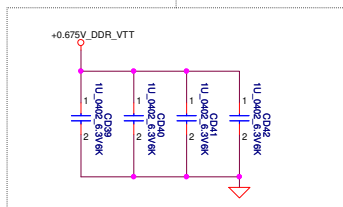
+V_DDR_REF, +SB_DIMM2_VREFDQ, +SB_DIMM_VREFDQ, +DIMM2_VREF_DQ
traces should be at least 20 mils wide and 20 mils spacing to other signals /planes.



Layout Note:
Place near JDIMM2



Layout Note:
Place near JDIMM2.203,204



+V_DDR_REF, +SM_VREF_DIMM, +DIMM1_VREF_CA, +SM_VREF, +DIMM1_VREF_CA traces should be at least 20 mils wide and 20 mils spacing to other signals /planes.

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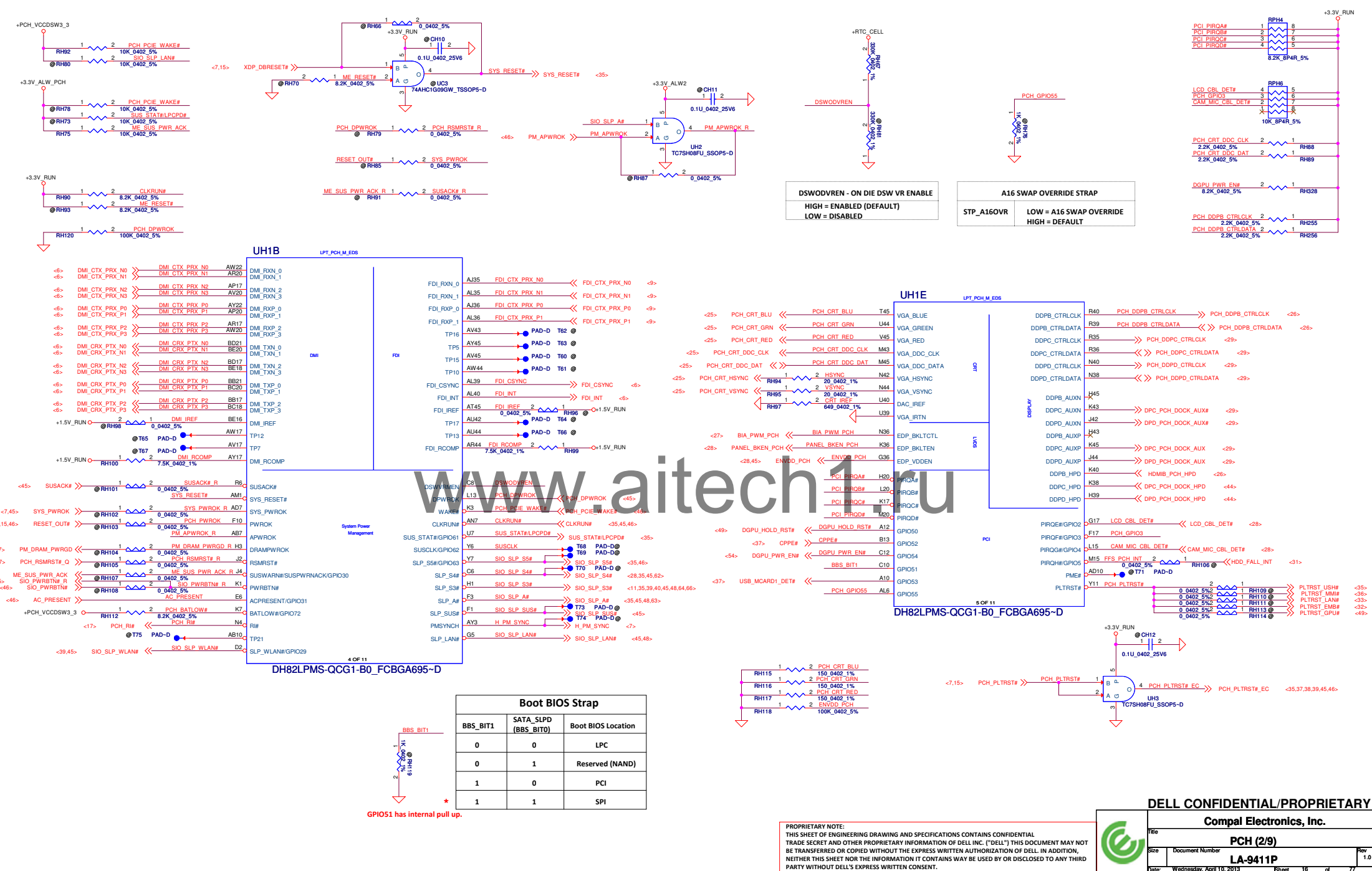
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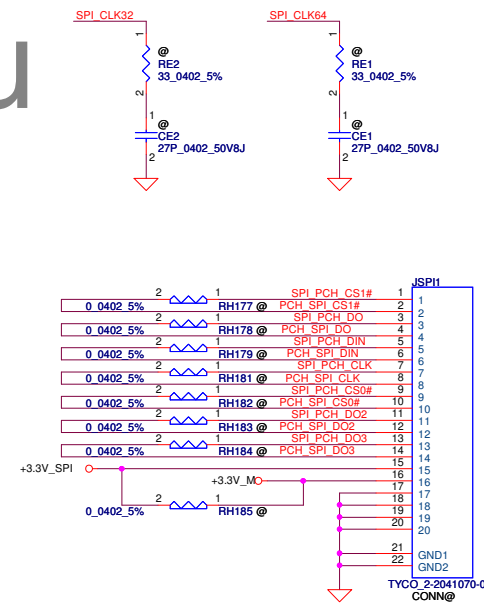
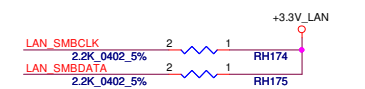
DDRIII-SODIMM SLOT2

LA-9411P

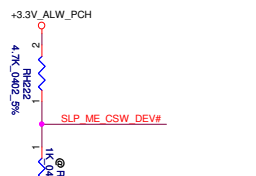
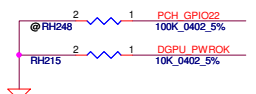
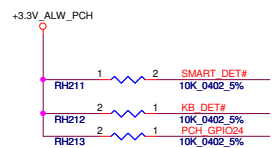
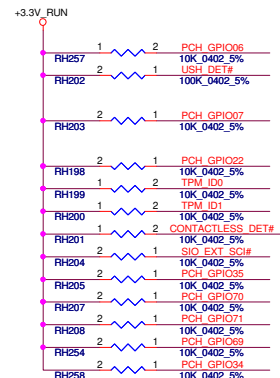
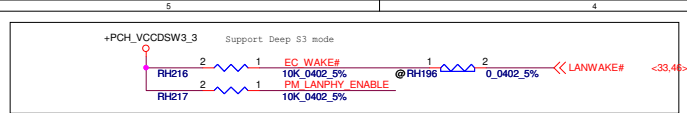
Rev
1.0

Date: Wednesday, April 10, 2013 Sheet 14 of 77

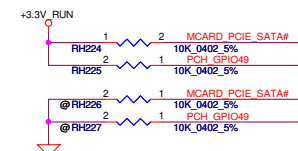




Date: Wednesday, April 10, 2013 Sheet 18 of 77



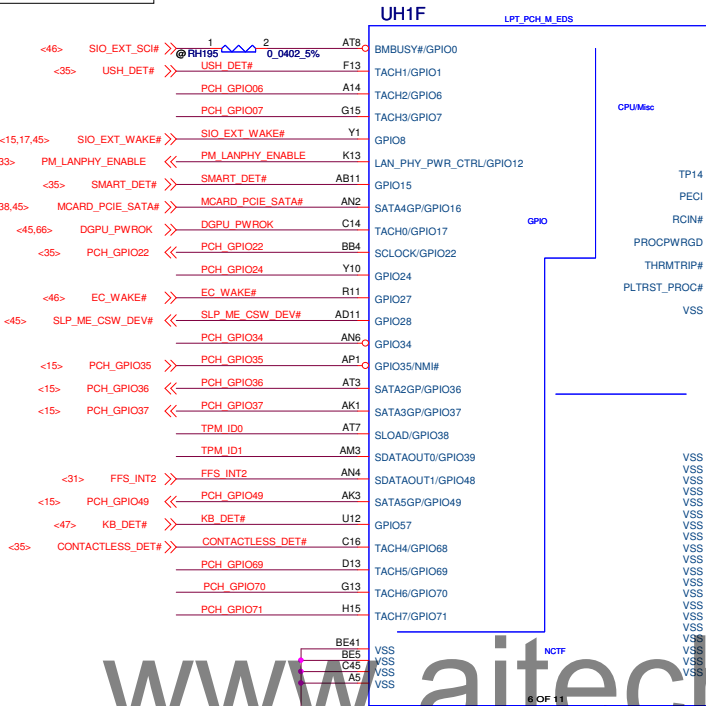
PLL ON DIE VR ENABLE
ENABLED - HIGH(DEFAULT)
DISABLED - LOW



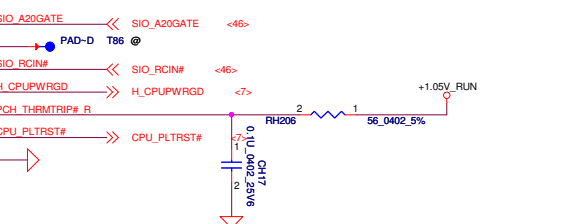
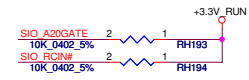
Config	GPIO16,49
USB X4,PCIEX8,SATAx6	11
USB X6,PCIEX8,SATAx4	01

*

Fixed Signals				Muxed Signals		Fixed Signals						Muxed Signals		Fixed Signals					
USB3 1	USB3 2	USB3 5	USB3 6	PCIE 1	PCIE 2	PCIE 3	PCIE 4	PCIE 5	PCIE 6	PCIE 7	PCIE 8	SATA 4	SATA 5	SATA 0	SATA 1	SATA 2	SATA 3		
				(00)	(00)							(00)	(00)						
				USB3 3	USB3 4							PCIE 1	PCIE 2						
				(01)	(01)							(01)	(01)						

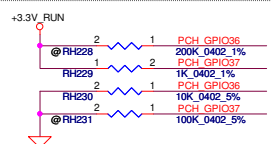


DH82LPM5 QCG1-B0_FCBGA695-D



CRB1.2 already change to GND directly at UH1.A44, B45, BD1 pins

PCH_GPIO37
0 = Disable Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality).
1 = Enable Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). Must be pulled up to support Intel AMT with TLS.



SATA2GP/GPIO36, SATA3GP/GPIO37 SAMPLED AT RISING EDGE OF PWROK.
WEAK INTERNAL PULL-DOWN.(WEAK INTERNAL PULL-DOWN IS DISABLED AFTER PLRST_N DE-ASSERTS).
NOTE: THIS SIGNAL SHOULD NOT BE PULLED HIGH WHEN STRAP IS SAMPLED.

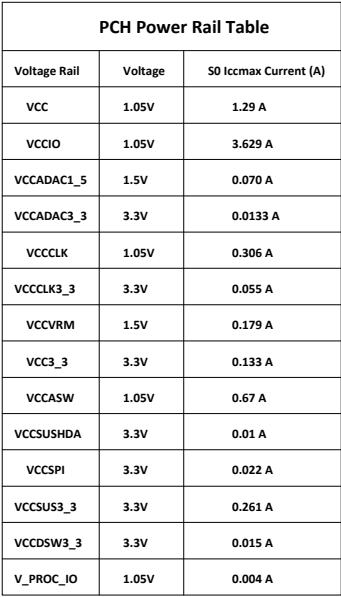
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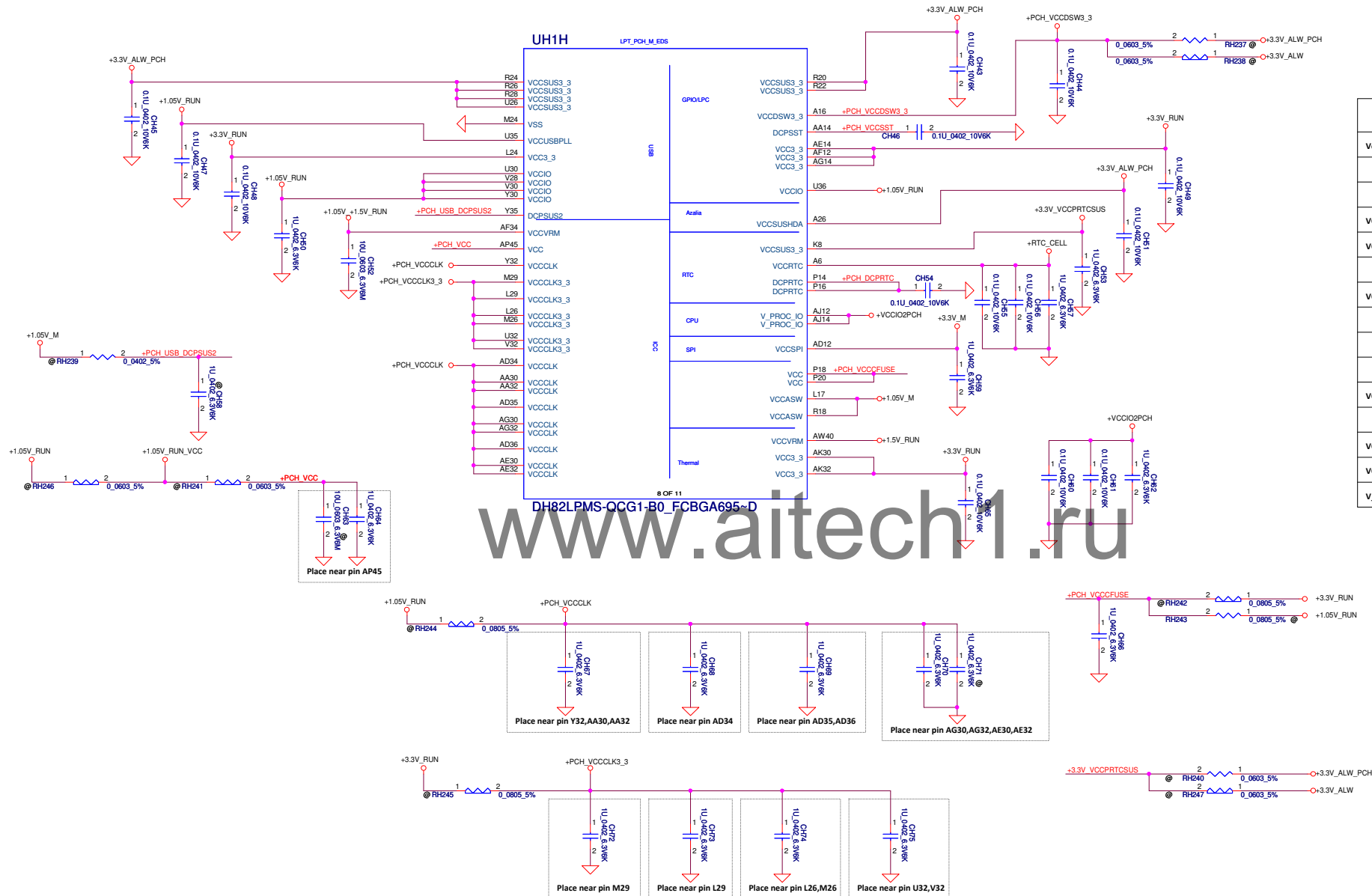
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Size	Document Number LA-9411P			
Date:	Wednesday, April 10, 2013	Sheet	20 of 77	

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	LA-9411P	1.0	
Date:	Wednesday, April 10, 2013	Sheet	21 of 77

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PCH Power Rail Table		
Voltage Rail	Voltage	50 Iccmax Current (A)
VCC	1.05V	1.29 A
VCCIO	1.05V	3.629 A
VCCADACL_5	1.5V	0.070 A
VCCADACL_3	3.3V	0.0133 A
VCCCLK	1.05V	0.306 A
VCCCLK_3	3.3V	0.055 A
VCCVRM	1.5V	0.179 A
VCC3_3	3.3V	0.133 A
VCCASW	1.05V	0.67 A
VCCSUSHDA	3.3V	0.01 A
VCCSPI	3.3V	0.022 A
VCCSUS3_3	3.3V	0.261 A
VCCDSW3_3	3.3V	0.015 A
V_PROC_IO	1.05V	0.004 A

8 OF 11
DH82LPMS-QCG1-B0_FCBGA695~D

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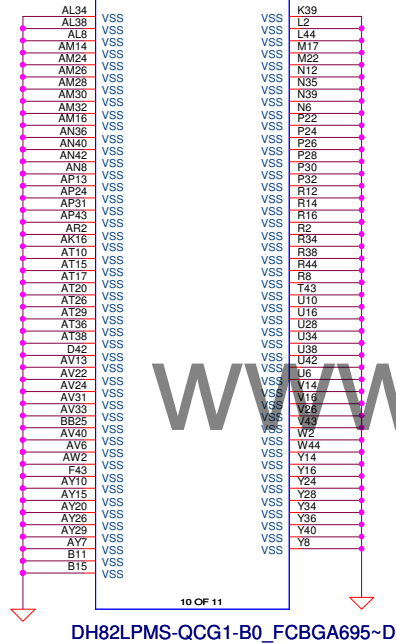
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Size	Document Number		Rev
	LA-9411P		1.0
Date:	Wednesday, April 10, 2013		Sheet 22 of 77

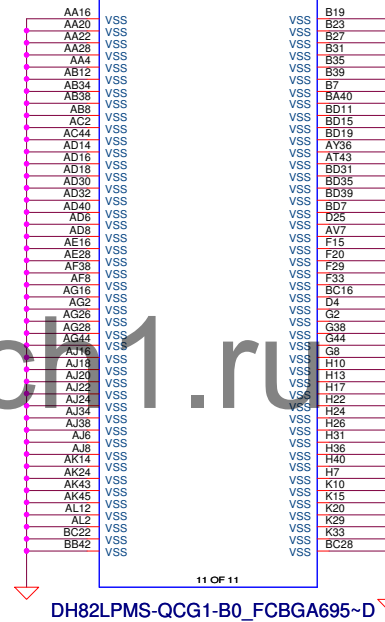
UH1J

LPT_PCH_M_EDS



UH1K

LPT_PCH_M_EDS



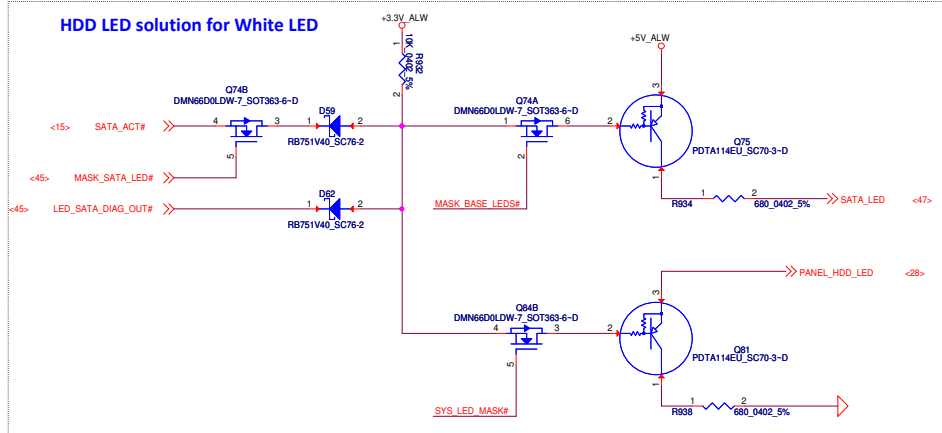
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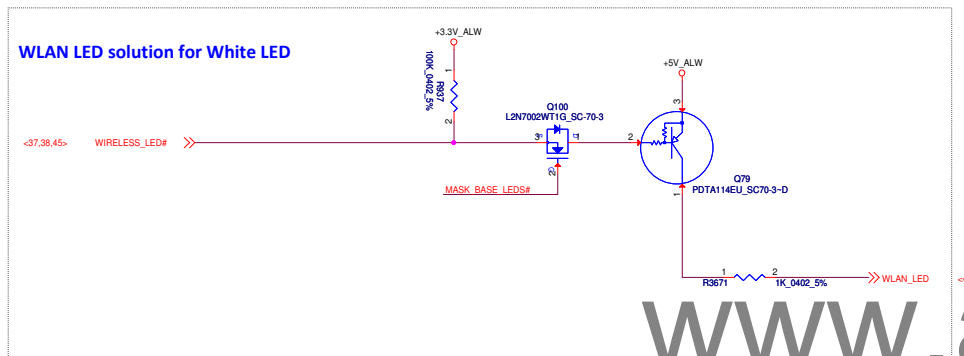
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Title			
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Size	Document Number		Rev
	LA-9411P		1.0
Date:	Wednesday, April 10, 2013		
	Sheet	23 of 77	

HDD LED solution for White LED

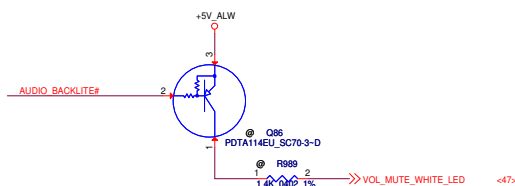
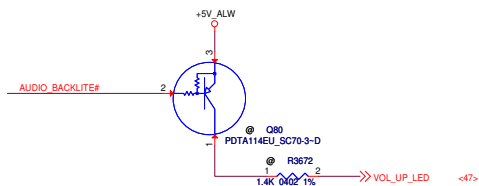


WLAN LED solution for White LED

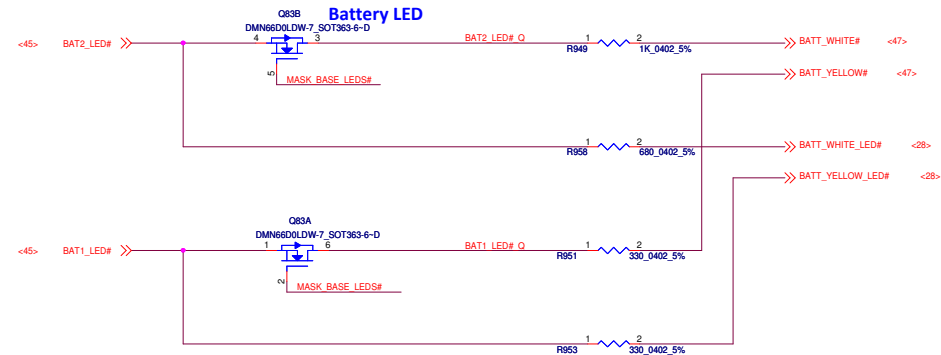


<45> AUDIO_BACKLITE# >>> 2 1.4k Q2 1% >>> VOL_DOWN_LED <47>

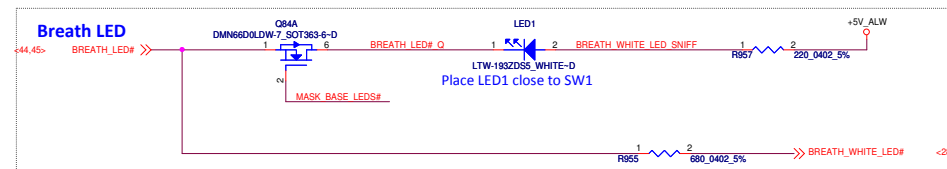
Q2 PDA114EU_SC70-3-D
 R954 1.4k Q2 1%



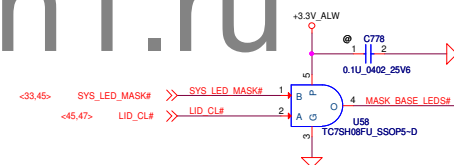
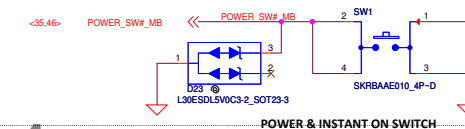
ery LED



Breath LED



PWR SW

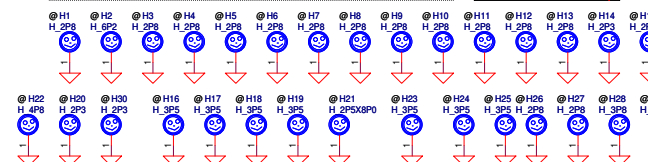
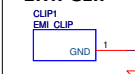


LED Circuit Control Table		
	SYS_LED_MASK#	LID_CL#
Mask All LEDs (Sniffer Function)	0	X
Mask Base MB LEDs (Lid Closed)	1	0
Do not Mask LEDs (Lid Opened)	1	1

Fiducial Mark



EMI CLIP



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PWR SW/LED/PAD/ME

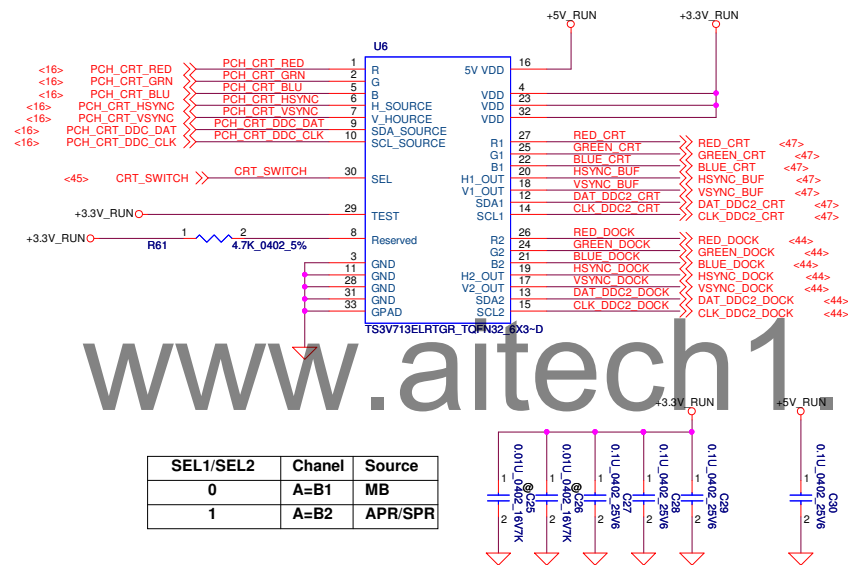
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SW for MB/DOCK

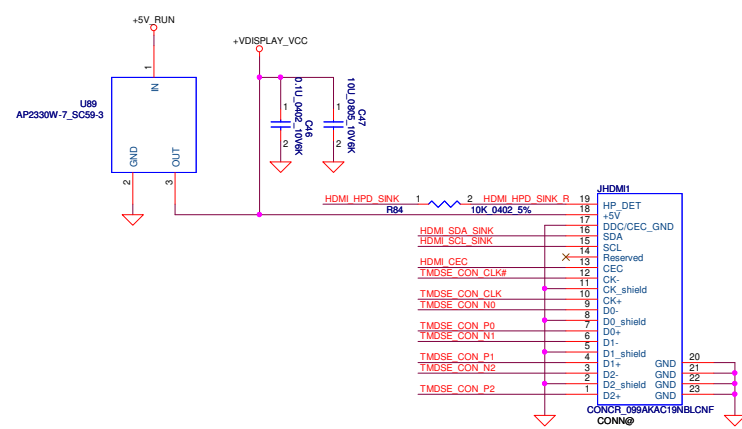
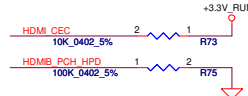
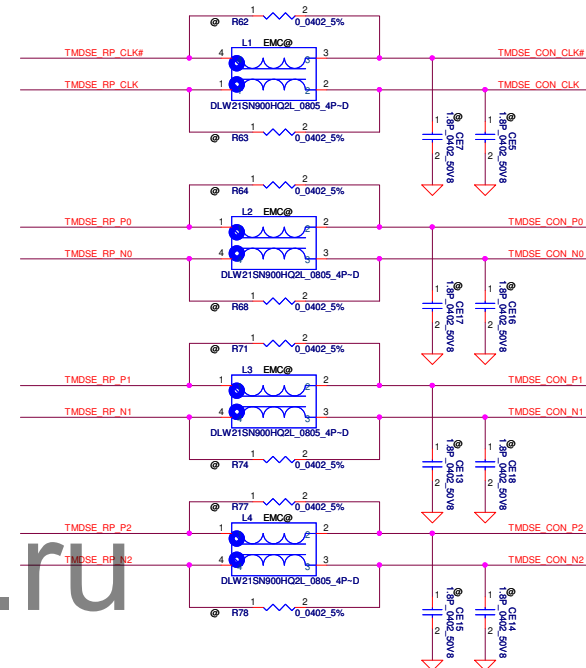
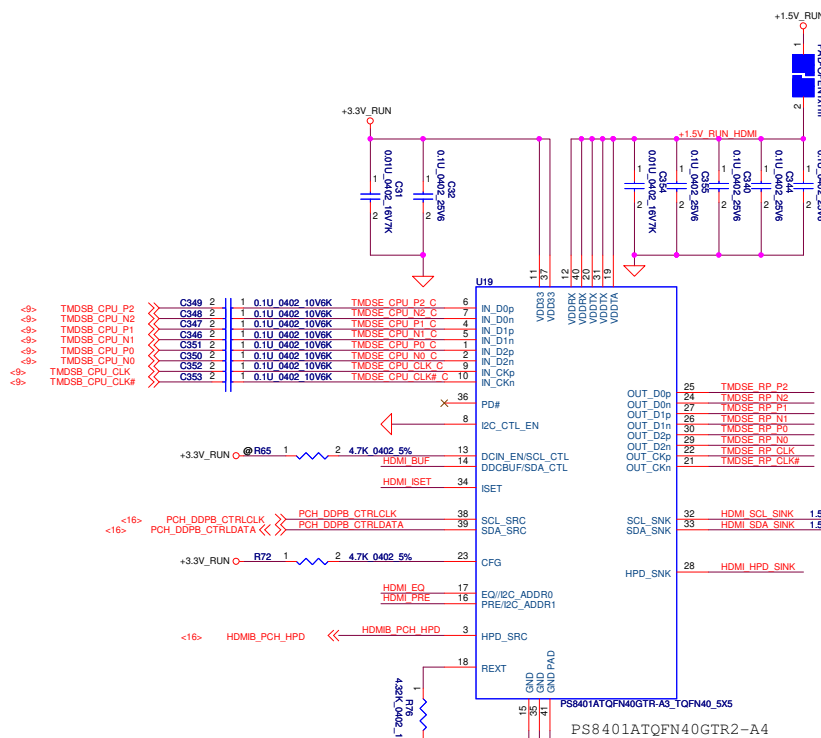


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Size	Document Number		Rev
	LA-9411P		1.0
Date:	Wednesday, April 10, 2013	Sheet	25 of 77



Enable active DDC buffer; Internal pull up at ~150kΩ, 3.3V I/O
 L: default, passive DDC pass-through
 H: active DDC buffer with default threshold
 M: passive DDC pass-through with internal ~10kΩ pull up

Receiver equalization setting; Internal pull down at ~150kΩ, 3.3V I/O.
 L: programmable EQ for channel loss up to 5.3dB
 H: programmable EQ for channel loss up to 10dB
 M: programmable EQ for channel loss up to 14dB

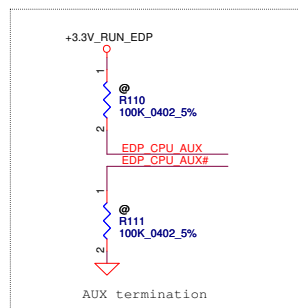
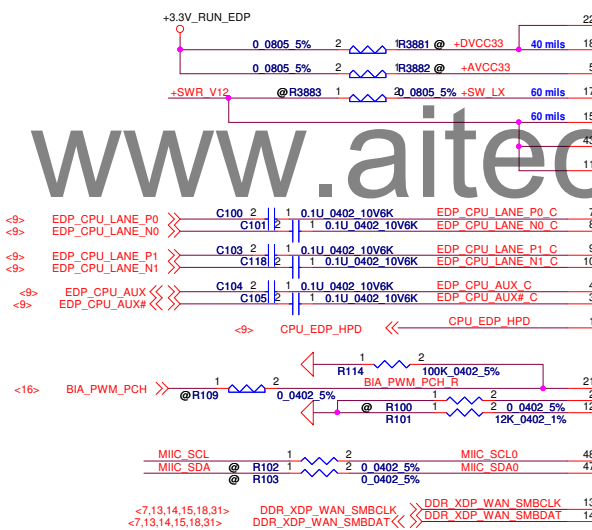
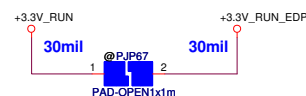
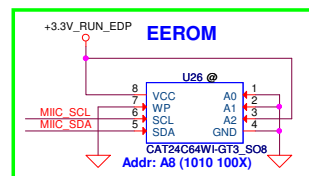
TMDs output swing adjustment; Internal pull down at ~150kΩ, 3.3V I/O.
 L: default
 H: increase +13%
 M: reduce -13%

Output pre-emphasis setting; Internal pull down at ~150kΩ, 3.3V I/O.
 L: no pre-emphasis
 H: 1.6dB pre-emphasis
 M: 3.0dB pre-emphasis

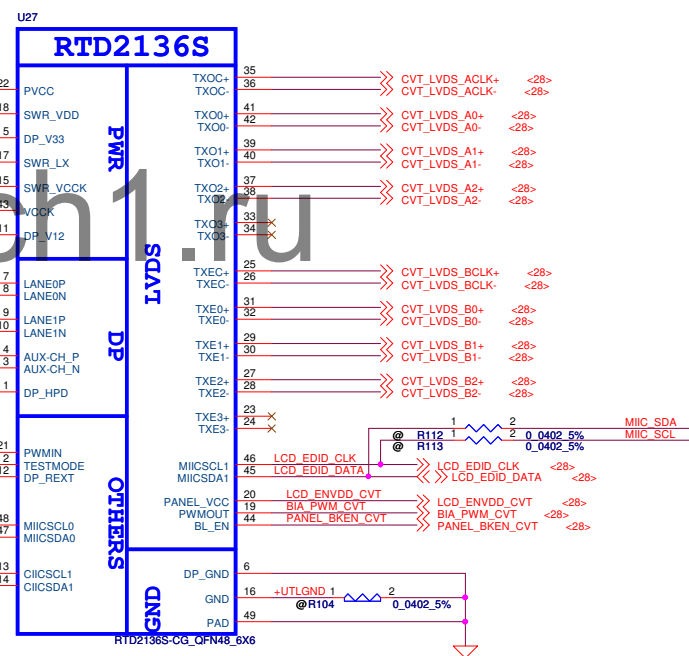
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File	HDMI CONN			Rev	1.0
Size	Document Number	LA-9411P			
Date	Wednesday, April 10, 2013	Sheet	26	of 77	



Pin5 (DPV33) < 20mA
Pin 11 (DPV12) < 100mA
Pin 15 (SWR_VCCK) < 100mA (layout trace > 60 mil)
Pin 17 (SWR_LX) < 600mA (layout trace > 60 mil)
Pin 18 (SWR_VDD) < 200mA (layout trace > 40 mil)
Pin 22 (PVCC) < 50 mA
Pin 43 (VCCK) < 50mA



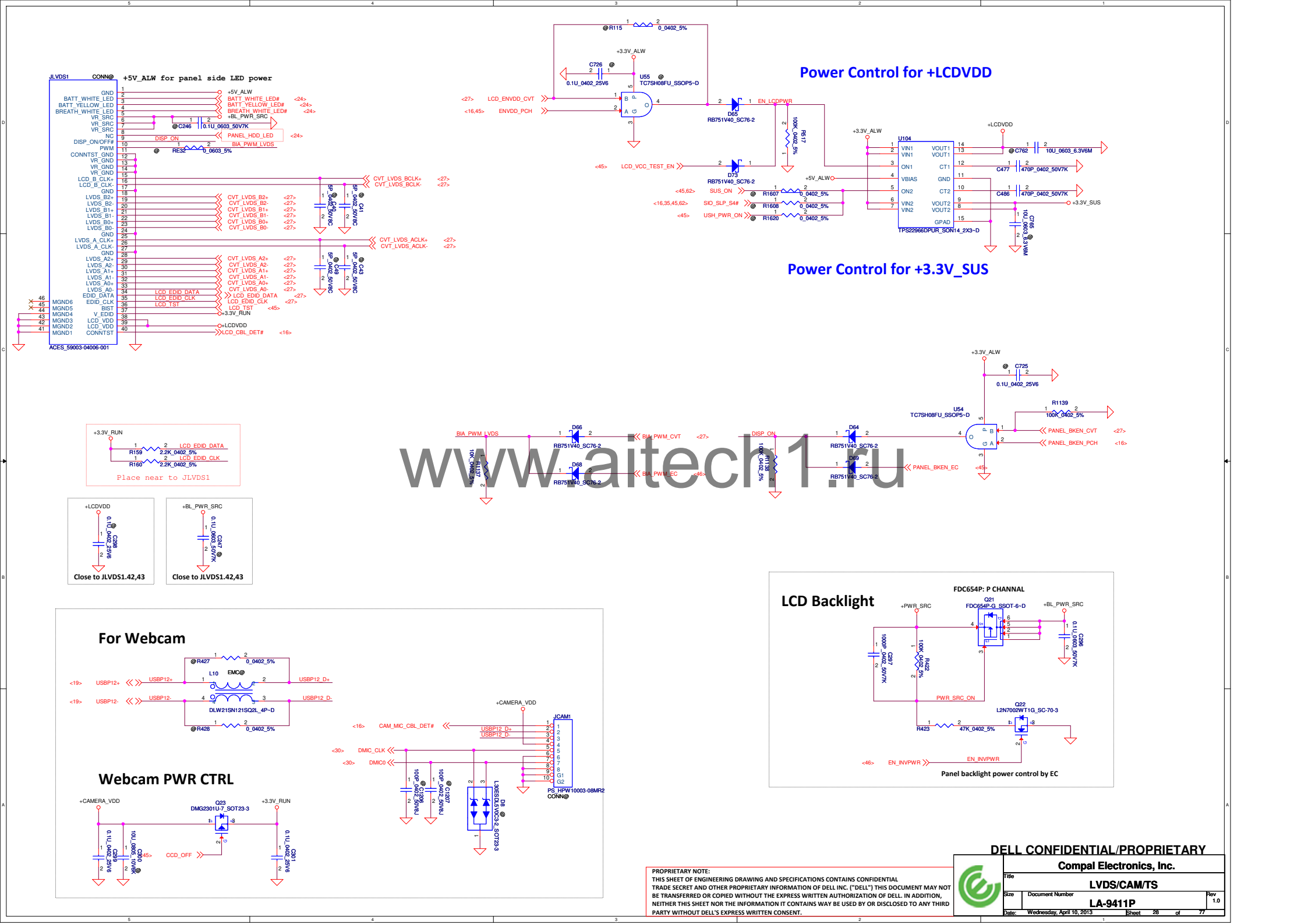
*** 1. RTD2136S:SA00004NW10 Populated R102, R103, R107; De-populated R108:
2. RTD2136R SA000067100 : De-Populated R102, R103, R107; Populate R108:

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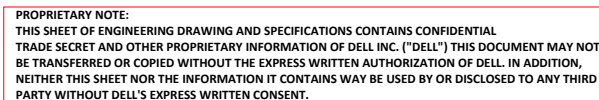


Rev	1.0
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Date: Wednesday, April 10, 2013 Sheet 27 of 77



AUX/DDC GPU for DPD to E-DOCK



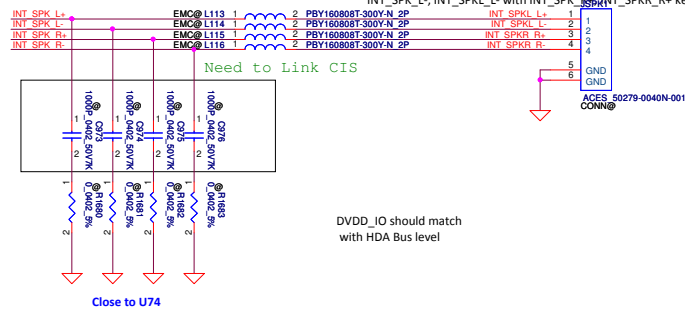
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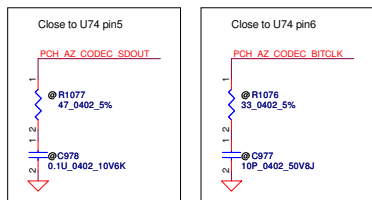
Size	Document Number	Rev
	LA-9411P	1.0
Date:	Wednesday, April 10, 2013	Sheet 29 of 77

Internal Speakers Header

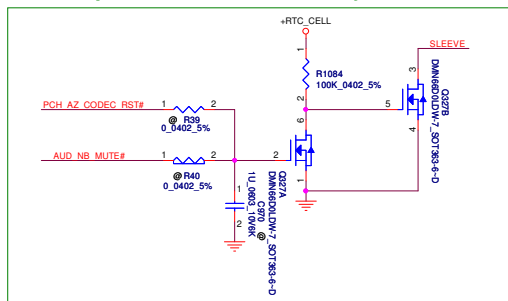
INT_SPK_L+, INT_SPK_L- :40 mils trace, keep 10mils spacing
INT_SPK_L-, INT_SPK_L- :40 mils trace, keep 10mils spacing
INT_SPK_R+, INT_SPK_R- :40 mils trace, keep 10mils spacing
INT_SPK_L-, INT_SPK_R- :40 mils trace, keep 10mils spacing
INT_SPK_L-, INT_SPK_L- with INT_SPK_R+ keep 20mils spacing



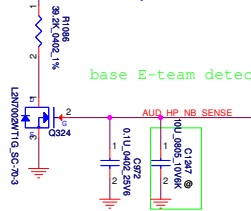
DVDD_IO should match with HDA Bus level



When no external power, it Sleeve will be floating mode and no reference GND.

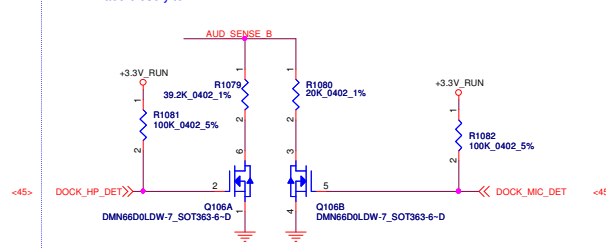


AUD SENSE A
Place closely to Pin 13.



Add for solve pop noise and detect issue

Place closely to Pin 14



<15> PCH_AZ_CODEC_BITCLK >> PCH_AZ_CODEC_BITCLK
<15> PCH_AZ_CODEC_SDOUT >> PCH_AZ_CODEC_SDOUT
<15> PCH_AZ_CODEC_SYNC >> PCH_AZ_CODEC_SYNC
<15> PCH_AZ_CODEC_SDOIN >> PCH_AZ_CODEC_SDOIN
<15> PCH_AZ_CODEC_RST# >> PCH_AZ_CODEC_RST#

<44> DAI_12MHZ# >> DAI_12MHZ#
<44> DAI_BCLK# >> DAI_BCLK#
<44> DAI_DO# >> DAI_DO#
<44> DAI_LRCK# >> DAI_LRCK#
<44> DAI_DI >> DAI_DI

BCLK: Audio serial data bus bit clock input/output
LRCK: Audio serial data bus word clock input/output

AUD_NB_MUTE# >> AUD_NB_MUTE#

AUD_NB_MUTE# >> AUD_NB_MUTE#

AUD_NB_MUTE# >> AUD_NB_MUTE#

AUD_NB_MUTE# >> AUD_NB_MUTE#

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AUD_NB_MUTE# >> AUD_NB_MUTE#

AUD_NB_MUTE# >> AUD_NB_MUTE#

RING2_L, RING2,
AUD_HP_OUT_L2, AUD_HP_OUT_L1, AUD_HP_OUT_L,
AUD_HP_OUT_R2, AUD_HP_OUT_R1, AUD_HP_OUT_R,
EXT_MIC, SLEEVE Trace width to 15mils.

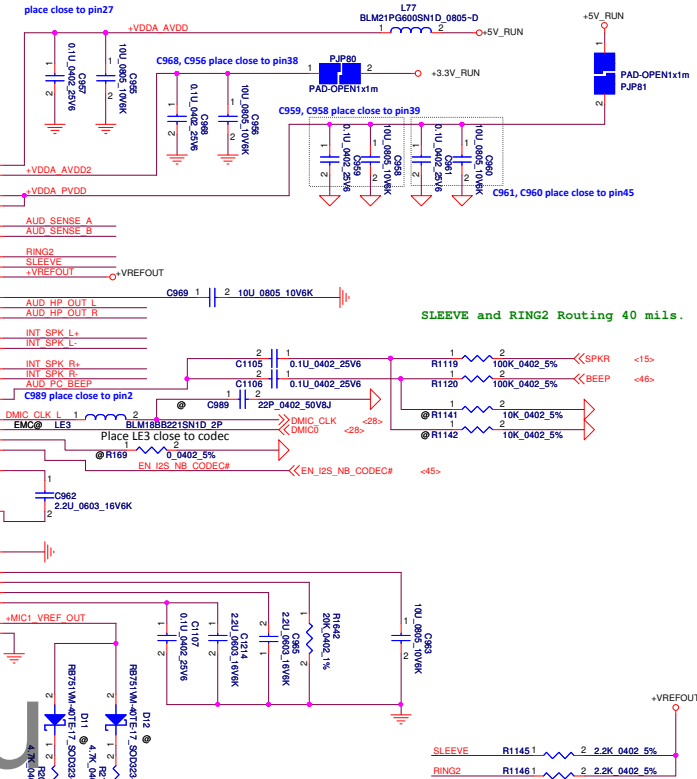
Resistor	SENSE_A	SENSE_B
39.2K	PORT A	PORT E
20K	PORT B	PORT F
10K	NA	DMIC0
5.11K	SPDIFOUT0	SPDIFOUT1 (DMIC1)
2.49K	Pull-up to AVDD	

Notes:
Keep PVDD supply and speaker traces routed on the DGND plane.
Keep away from AGND and other analog signals

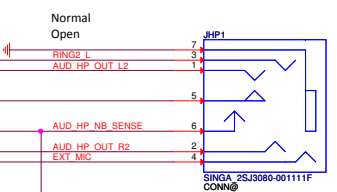
PORT A	External MIC
PORT B	HeadPhone Out
PORT C	Dock Audio
PORT D	Internal SPK

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support universal Jack

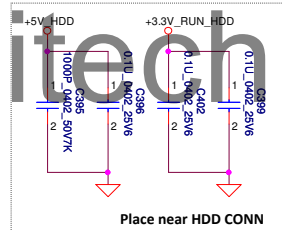
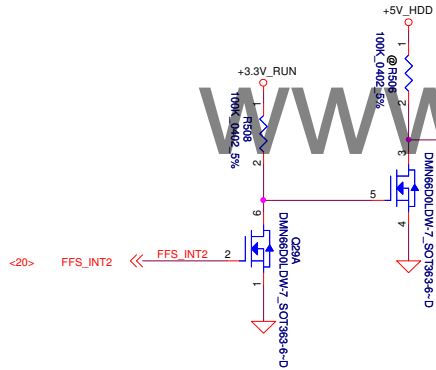
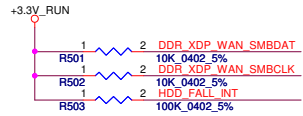
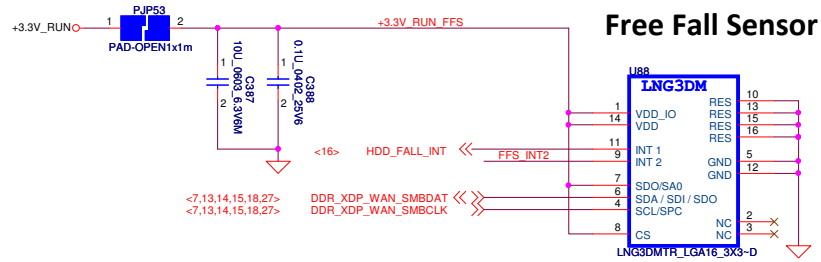


Combo Jack

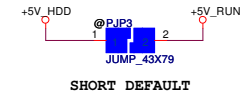


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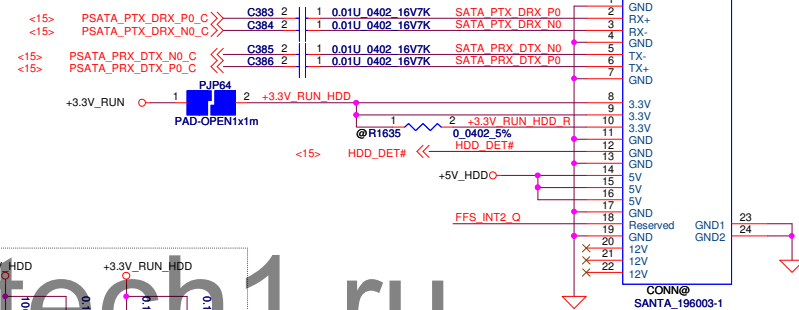
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Code			
Size	Document Number	Rev	1.0
	LA-9411P		
Date:	Wednesday, April 10, 2013	Sheet	30 of 77



HDD PWR



HDD CONN



Main SATA +5V Default

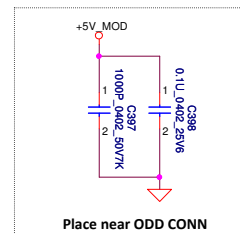
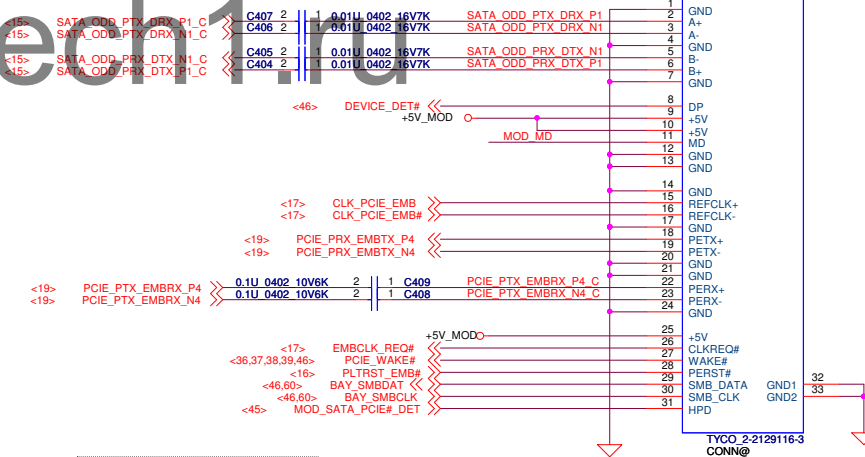
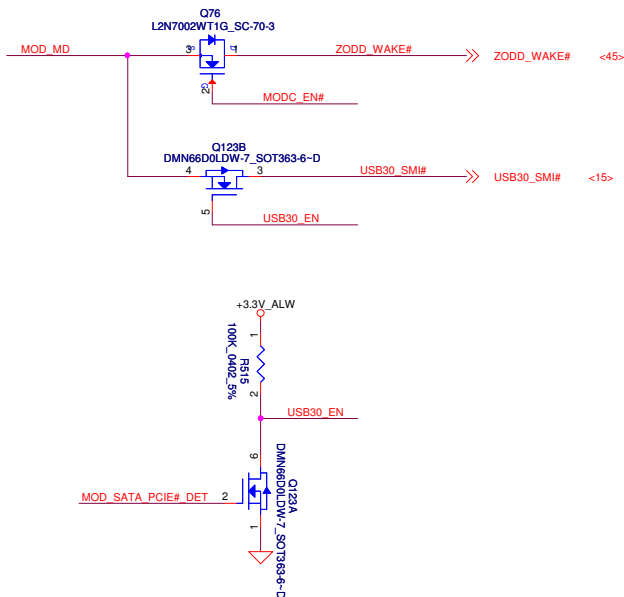
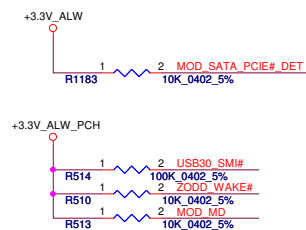
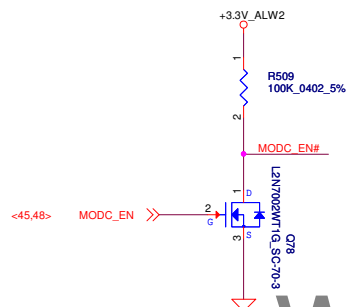
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HDD			Rev
Size	Document Number	LA-9411P	1.0
Date:	Wednesday, April 10, 2013	Sheet	31 of 77

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Place near ODD CONN

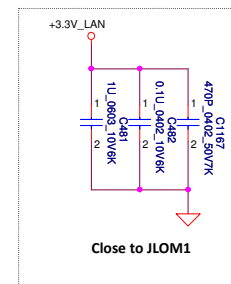
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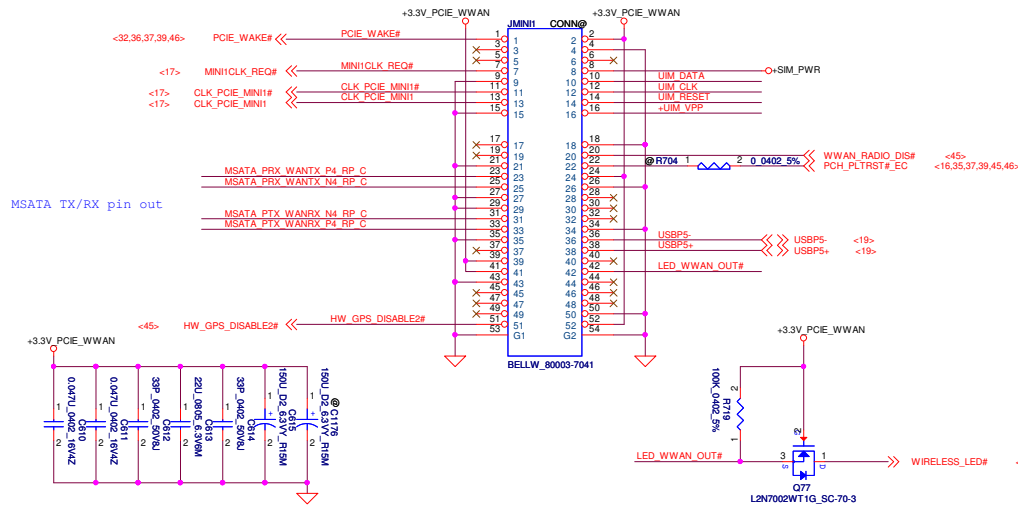
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Title		ODD	
Size	Document Number	LA-9411P	
Date:	Wednesday, April 10, 2013	Sheet	32 of 77
Rev	1.0		





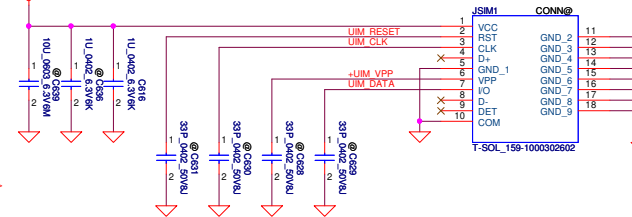
Mini WWAN/GPS/LTE/UWB H=9



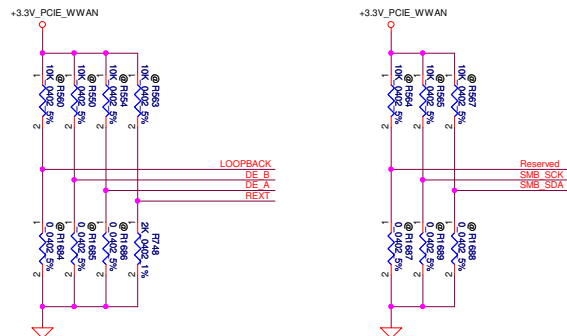
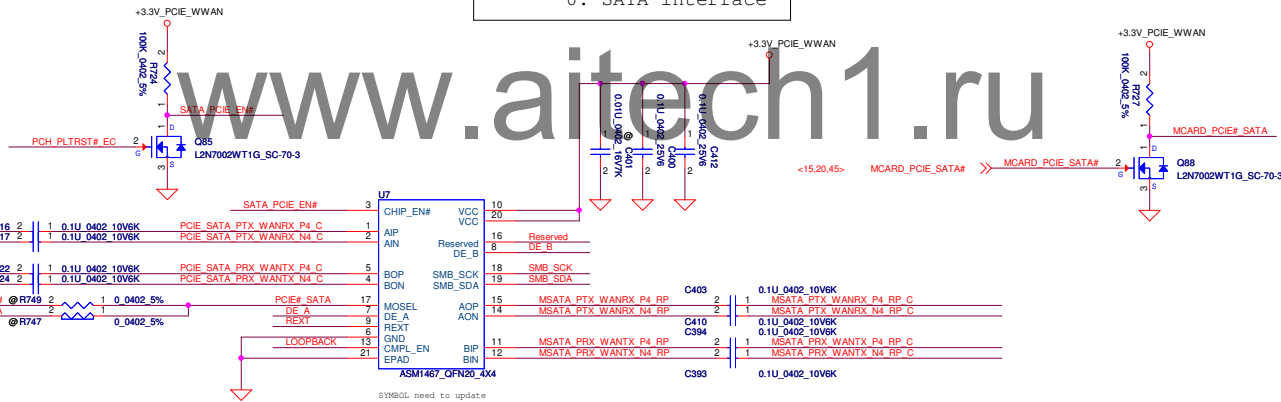
- Wake Enabled and Active
- Wake NOT Enabled nor Active

PWR Rail	Voltage Tolerance	D0-D2&D3 hot Power		D3 cold Power	
		Peak (mA)	Typ (mA)	Peak (mA)	Typ (mA)
+3.3V_PCIE_WWAN	+/-9%	2750	800	800 (1)	150 (1) 5 (2)

SIM Card Push-Push



MOSEL 1: PCIE interface
0: SATA interface



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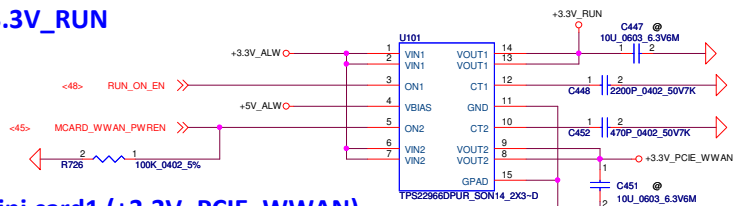
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WWAN Mini Card

Title	Document Number	Rev
LA-9411P	1.0	
Date: Wednesday, April 10, 2013	Sheet 38 of 77	

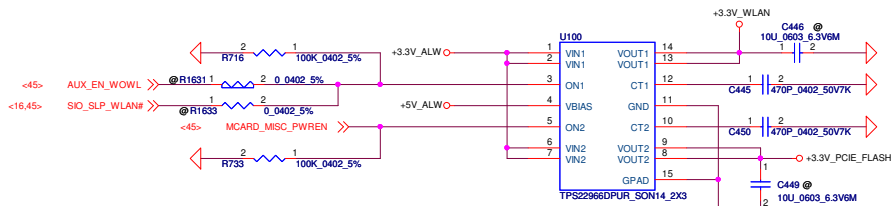
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Power Control for +3.3V_RUN



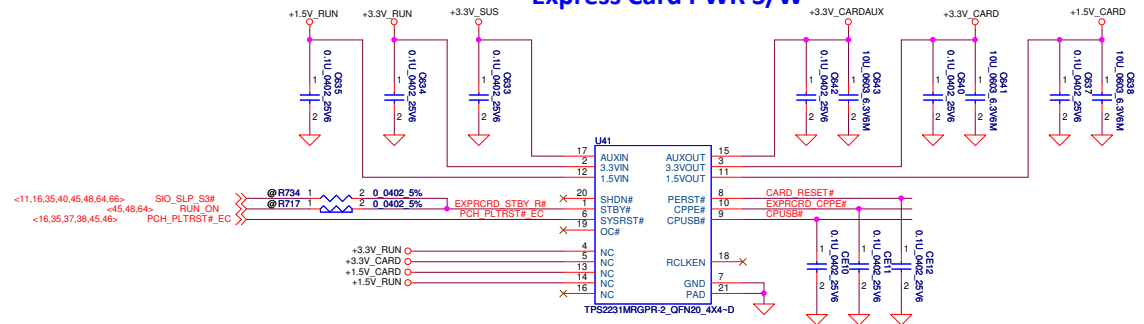
Power Control for Mini card1 (+3.3V_PCIE_WWAN)

Power Control for Mini card2 (+3.3V_WLAN)



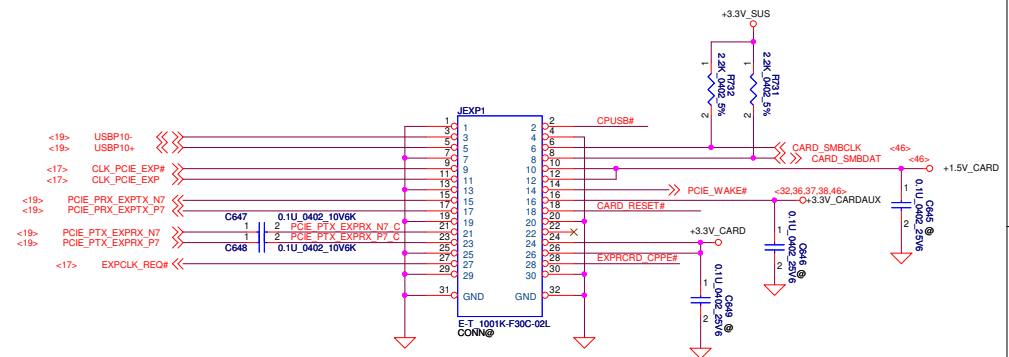
Power Control for Mini card3 (+3.3V_PCIE_FLASH)

Express Card PWR S/W



Express Card Conn.

Note: Add connection on pin4, pin5, pin 13 and pin14 to support GMT 2nd source part



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PCIE-SATA SW / PCIE PWR

LA-9411P

Date: Wednesday, April 10, 2013 Sheet 39 of 77

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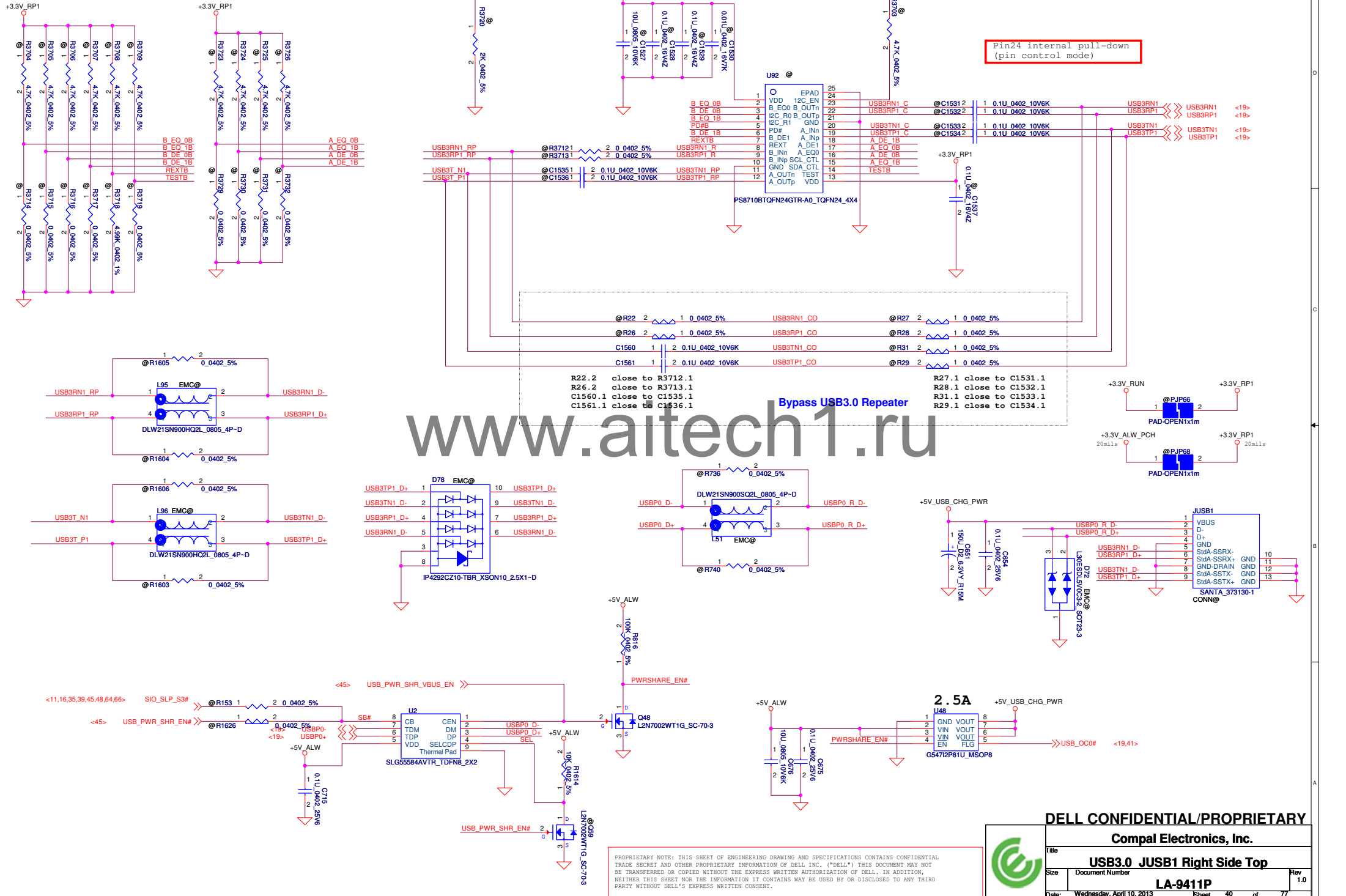
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Right Side Top (JUSB1)

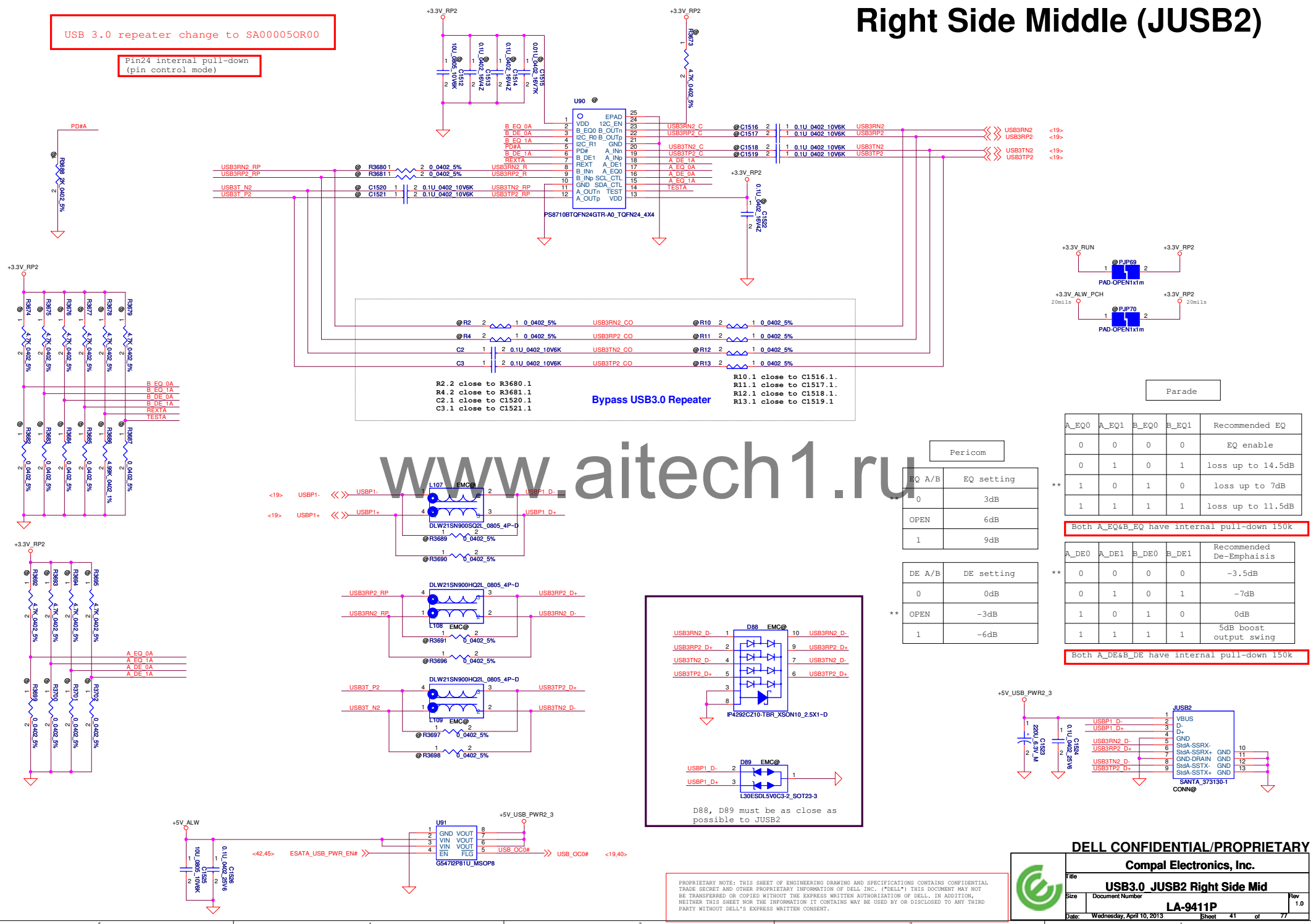
USB 3.0 repeater change to SA000050R00

Pin24 internal pull-down
(pin control mode)



USB 3.0 repeater change to SA000050R00

Pin24 internal pull-down
(pin control mode)



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USB3.0 JUSB2 Right Side Mid

LA-9411P

Date: Wednesday, April 10, 2013 Sheet 41 of 77

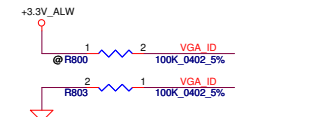
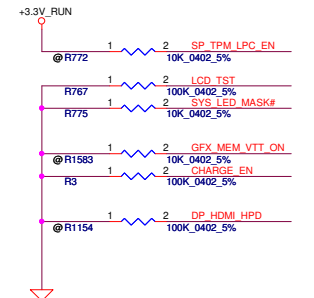
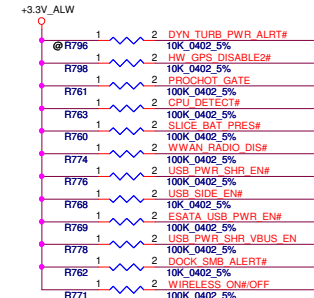
USB 3.0 repeater change to SA000050R00

```

C1564 1 2 01U_0402 10V6K USB3_R3_00 @P36
C1564 1 2 01U_0402 10V6K USB3_R5_00 @P36
R32.2 close to R3770.1
R33.2 close to R3763.1
C1563.1 close to C1551.1
C1564.1 close to C1533.1

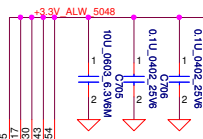
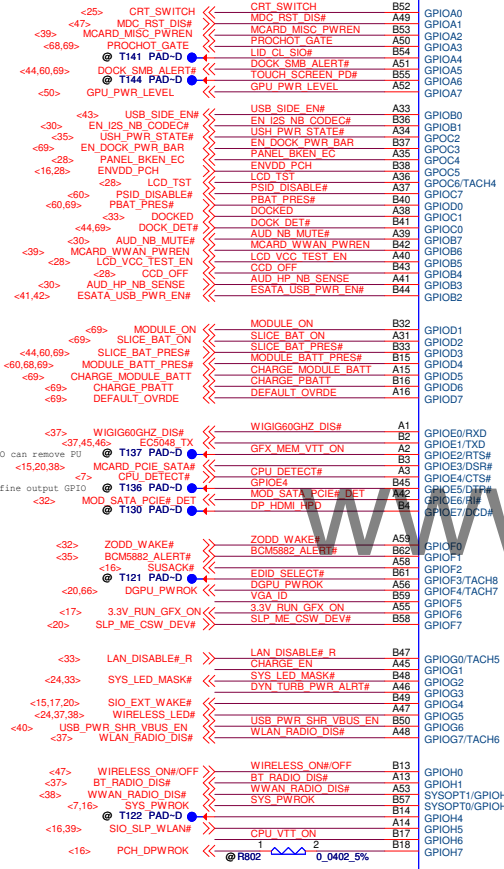
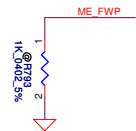
```

Rev
4.0

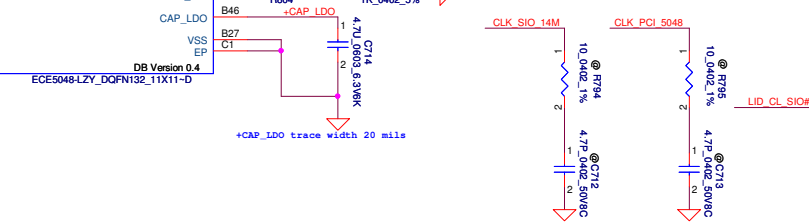
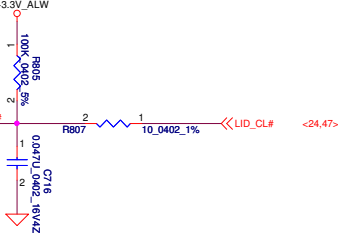
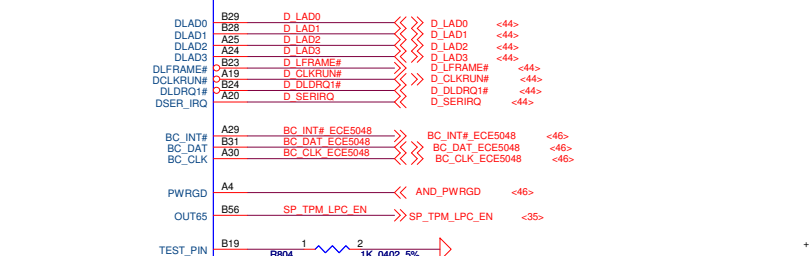
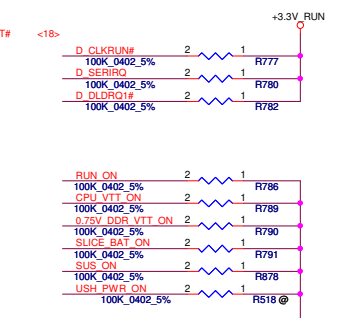
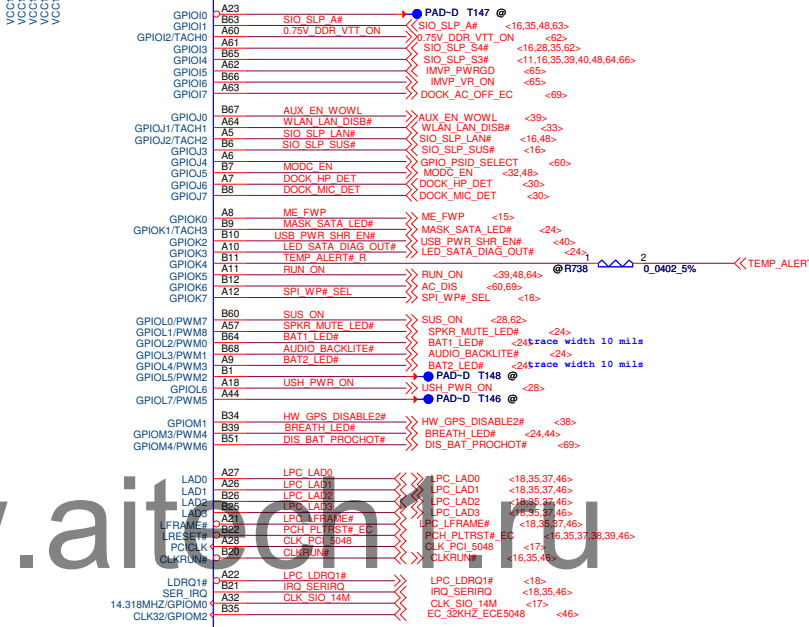


	VGA_ID0
Discrete	0
UMA	1

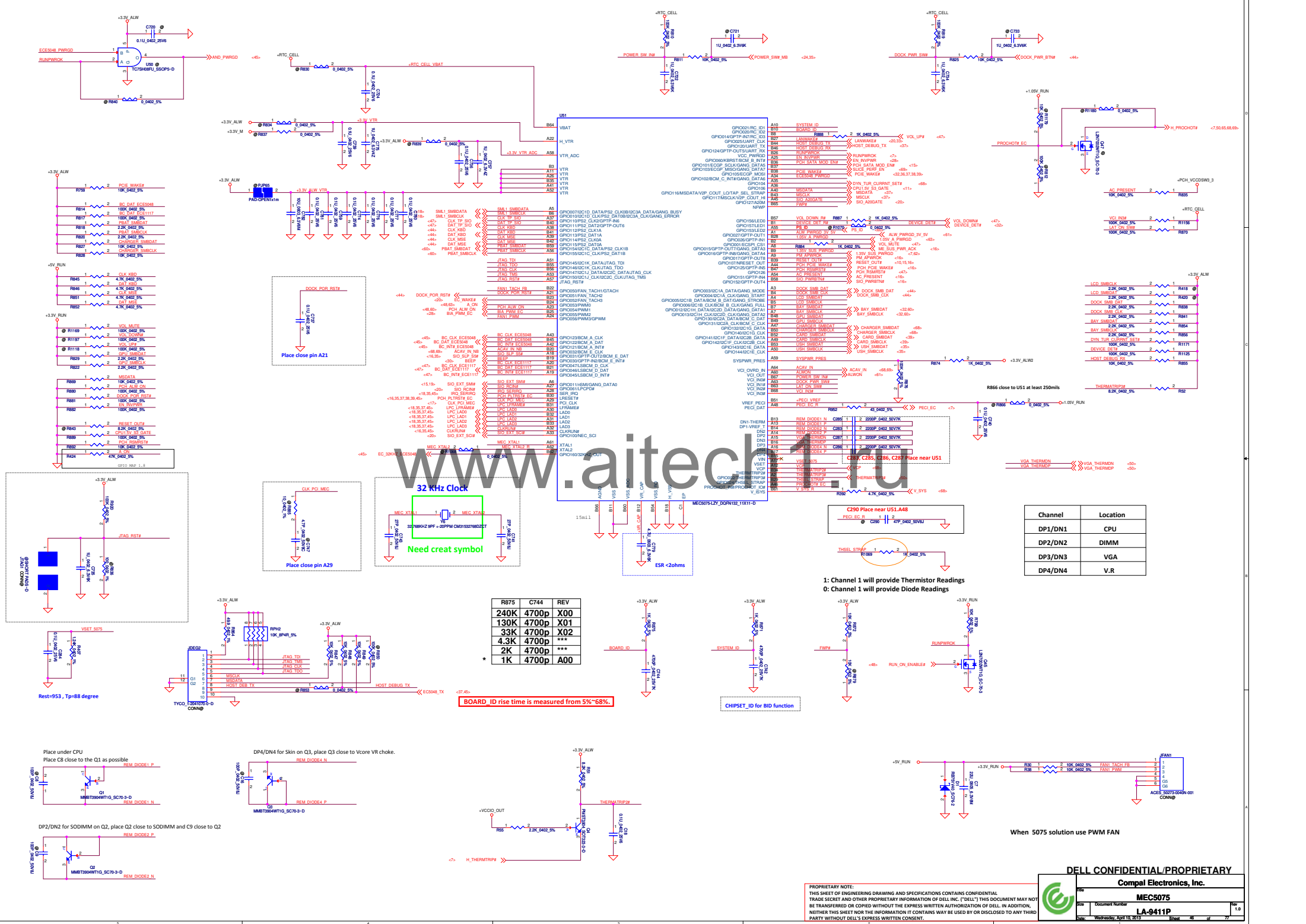
ME_FWP PCH has internal 20K PD.



SMSC feedback disconnect LPC_LDRQ0# at A23 pin



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Channel	Location
DP1/DN1	CPU
DP2/DN2	DIMM
DP3/DN3	VGA
DP4/DN4	V.R

1: Channel 1 will provide Thermistor Readings
0: Channel 1 will provide Diode Readings

R875	C744	REV
240K	4700p	X00
130K	4700p	X01
33K	4700p	X02
4.3K	4700p	***
2K	4700p	A00

BOARD_ID rise time is measured from 5%~68%.

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Compal Electronics, Inc.	
MEC5075	
Document Number	LA-9411P
Web	Wednesday, April 16, 2013
Sheet	46 of 77

<6> PEG_CTX_GRX_P[0..7] >> PEG_CTX_GRX_N[0..7]
 <6> PEG_CTX_GRX_N[0..7] >> PEG_CTX_GRX_P[0..7]
 <6> PEG_CRX_GTX_P[0..7] >> PEG_CRX_GTX_N[0..7]
 <6> PEG_CRX_GTX_N[0..7] >> PEG_CRX_GTX_P[0..7]

PEG_CRX_GTX_P0	15G@	CV1	2	1	0.22U	0402	16V7K	PEG_CRX_GTX_C_P0
PEG_CRX_GTX_N0	15G@	CV2	2	1	0.22U	0402	16V7K	PEG_CRX_GTX_C_N0
PEG_CRX_GTX_P1	15G@	CV4	2	1	0.22U	0402	16V7K	PEG_CRX_GTX_C_P1
PEG_CRX_GTX_N1	15G@	CV3	2	1	0.22U	0402	16V7K	PEG_CRX_GTX_C_N1
PEG_CRX_GTX_P2	15G@	CV5	2	1	0.22U	0402	16V7K	PEG_CRX_GTX_C_P2
PEG_CRX_GTX_N2	15G@	CV6	2	1	0.22U	0402	16V7K	PEG_CRX_GTX_C_N2
PEG_CRX_GTX_P3	15G@	CV7	2	1	0.22U	0402	16V7K	PEG_CRX_GTX_C_P3
PEG_CRX_GTX_N3	15G@	CV8	2	1	0.22U	0402	16V7K	PEG_CRX_GTX_C_N3
PEG_CRX_GTX_P4	15G@	CV9	2	1	0.22U	0402	16V7K	PEG_CRX_GTX_C_P4
PEG_CRX_GTX_N4	15G@	CV10	2	1	0.22U	0402	16V7K	PEG_CRX_GTX_C_N4
PEG_CRX_GTX_P5	15G@	CV11	2	1	0.22U	0402	16V7K	PEG_CRX_GTX_C_P5
PEG_CRX_GTX_N5	15G@	CV12	2	1	0.22U	0402	16V7K	PEG_CRX_GTX_C_N5
PEG_CRX_GTX_P6	15G@	CV14	2	1	0.22U	0402	16V7K	PEG_CRX_GTX_C_P6
PEG_CRX_GTX_N6	15G@	CV15	2	1	0.22U	0402	16V7K	PEG_CRX_GTX_C_N6
PEG_CRX_GTX_P7	15G@	CV16	2	1	0.22U	0402	16V7K	PEG_CRX_GTX_C_P7
PEG_CRX_GTX_N7	15G@	CV17	2	1	0.22U	0402	16V7K	PEG_CRX_GTX_C_N7

PEG_CTX_GRX_P0 AA38 PCIE_RX0P
 PEG_CTX_GRX_N0 Y37 PCIE_RX0N
 PEG_CTX_GRX_P1 Y35 PCIE_RX1P
 PEG_CTX_GRX_N1 W36 PCIE_RX1N
 PEG_CTX_GRX_P2 W38 PCIE_RX2P
 PEG_CTX_GRX_N2 V37 PCIE_RX2N
 PEG_CTX_GRX_P3 V35 PCIE_RX3P
 PEG_CTX_GRX_N3 U36 PCIE_RX3N
 PEG_CTX_GRX_P4 U38 PCIE_RX4P
 PEG_CTX_GRX_N4 T37 PCIE_RX4N
 PEG_CTX_GRX_P5 T35 PCIE_RX5P
 PEG_CTX_GRX_N5 R36 PCIE_RX5N
 PEG_CTX_GRX_P6 R38 PCIE_RX6P
 PEG_CTX_GRX_N6 P37 PCIE_RX6N
 PEG_CTX_GRX_P7 P35 PCIE_RX7P
 PEG_CTX_GRX_N7 N36 PCIE_RX7N

PCI EXPRESS INTERFACE

CLOCK

PCIE_REFCLKP
 PCIE_REFCLKN

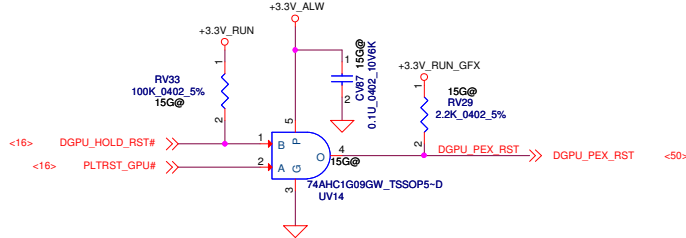
TEST_PG

PERSTB

MARS-PRO_FCBGA962-D

<17> CLK_PCIE_VGA >> AB35
 <17> CLK_PCIE_VGA# >> AA38
 15G@ RV25 1 2 1K_0402_5% AH16
 DGPU_PEX_RST 1 2 0_0402_5% @ RV18
 DGPU_PEX_RST# AA30

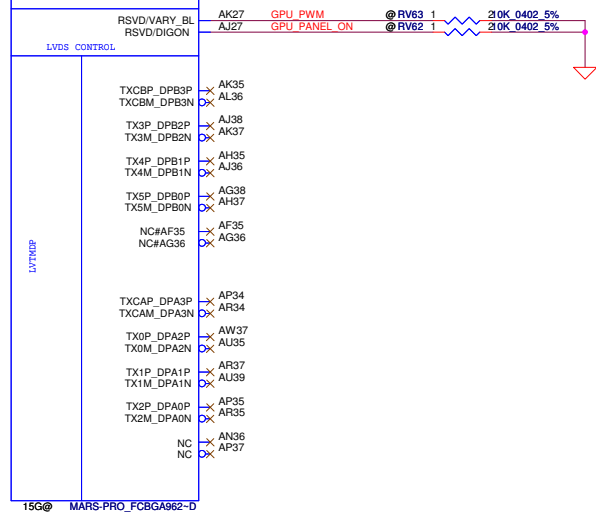
don't connect to PCH



PCIE_CALR_TX Y30 15G@ RV296 1 2 1.69K_0402_1% +VGA_PCIE
 PCIE_CALR_RX Y29 15G@ RV298 1 2 1K_0402_1% +VGA_PCIE

UV1A
 PART 1 OF 9

UV1D
 PART 7 OF 9



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MARX-PCIE

LA-9411P

Date: Wednesday, April 10, 2013 Sheet 49 of 77

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CONFIGURATION STRAPS

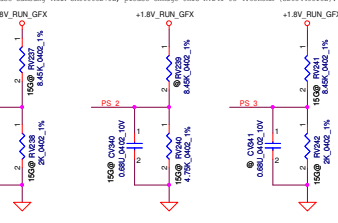
ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	RECOMMENDED SETTINGS	RECOMMENDED SETTINGS
TX_PWRS_ENB	GPIO0	POE FULL TX OUTPUT SWING	0: 50% swing 1: full swing	X
TX_DEEMPH_EN	GPIO1	POE TRANSMITTER DE-EMPHASIS	0: disable 1: enable	X
RSVD	GPIO2	Advertises PCIe speed when compliance test	0: 2.5GT/s 1: 5GT/s	0
RSVD	GPIO8	RESERVED		0
BF_VGA_ENB	GPIO9	VGA ENABLED		0
RSVD	GPIO21	RESERVED		0
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM	0: disable 1: enable	X
ROMIDCFG(2:0)	GPIO(13:11)	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT		XXX
VP_DEVICE_STRAP_ENA	VS2SYNC	IGNORE VIP DEVICE STRAPS		0
RSVD	HS2SYNC			0
RSVD	GENERICC			0
ALUD[1]	HS2SYNC	AD[0][1] AD[0][0] 0: 0.0 Hz audio function 1: 1.0 Hz audio function		11
ALUD[0]	VS2SYNC	0: 0.0 Hz audio function 1: 1.0 Hz audio function		11

AMD RESERVED CONFIGURATION STRAPS
ALLOW FOR PULLUP PADS FOR THESE STRAPS BUT DO NOT INSTALL RESISTOR. IF THESE GPIOs ARE USED, THEY MUST KEEP "LOW" AND NOT CONFLICT DURING RESET

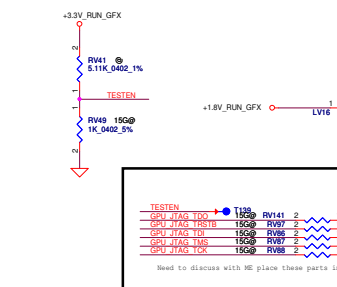
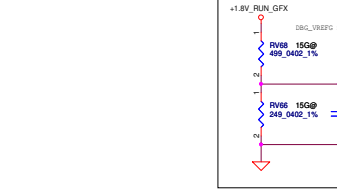
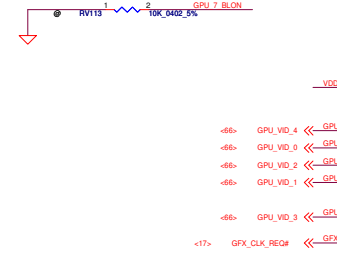
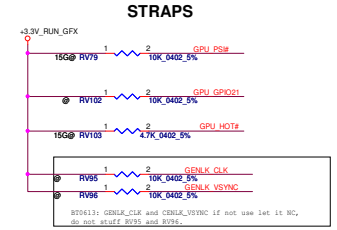
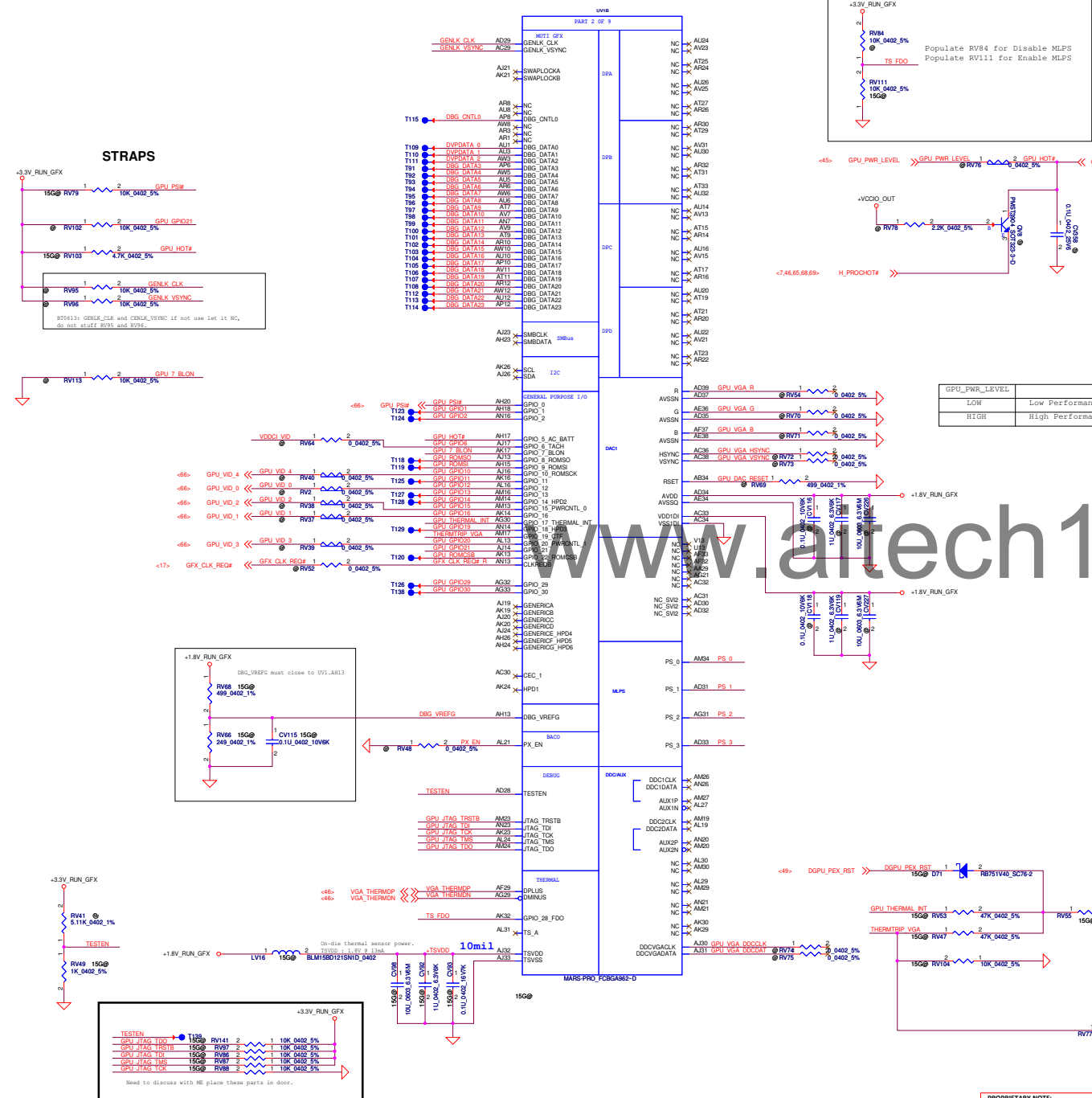
GPIO21	HS2SYNC	GENERICC	GPIO2	GPIO8
--------	---------	----------	-------	-------

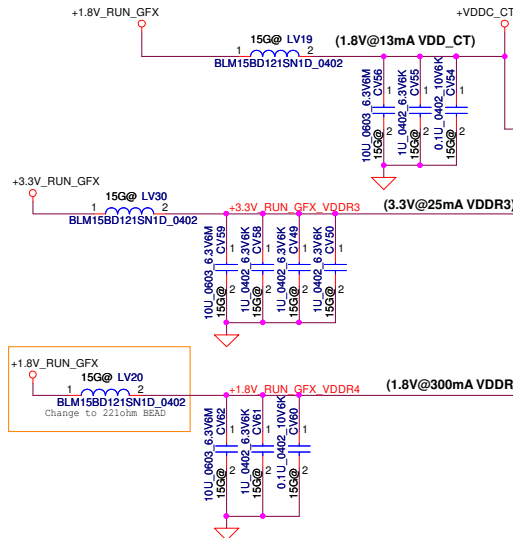
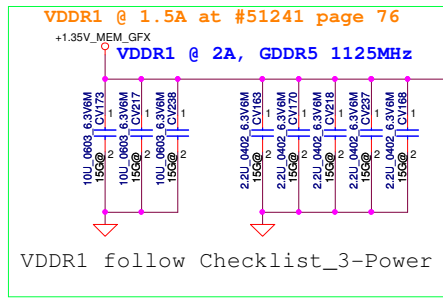
PS_3_1(3:2:1) For MEMB	RV241_PU	RV242_PU	CV341
001: N/A	RV241_PU	RV242_PU	CV341
010: Samsung K4D2032200 (1.35V)	8.45K	2K	NC
011: Samsung K4D2032200 (1.35V)	4.53K	2K	NC



TX_PWRS_ENB	GPIO0	Transmitter Power Saving Enable 0: 50% Tx output swing for mobile mode 1: full Tx output swing for Desktop
TX_DEEMPH_EN	GPIO1	PCI Express Transmitter De-emphasis Enable 0: Tx de-emphasis disabled for mobile mode 1: Tx de-emphasis enabled (Default setting for desktop)

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GPU_VDD_SENSE/GPU_VSS_SENSE route as differential pair

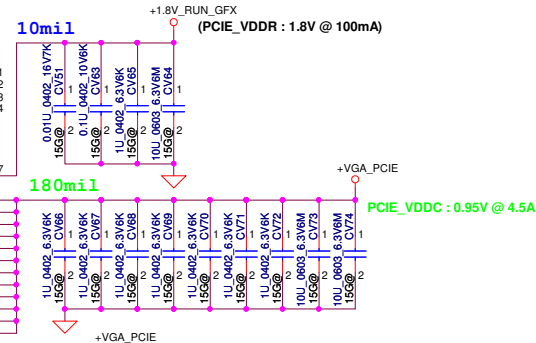
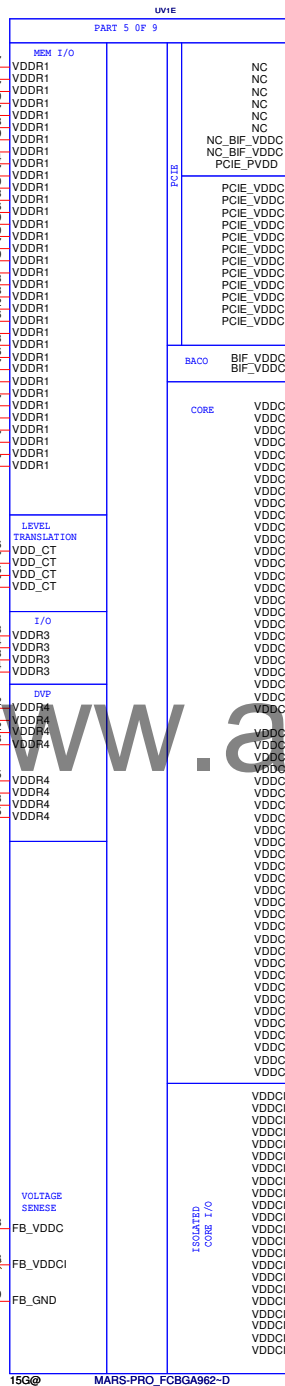
<66> GPU_VDD_SENSE >> GPU_VDD_SENSE

<66> GPU_VSS_SENSE >> GPU_VSS_SENSE

10mil

10mil

20mil



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Title	MARX-Power		
Size	Document Number	Rev	
	LA-9411P	1.0	
Date:	Wednesday, April 10, 2013	Sheet	51 of 77

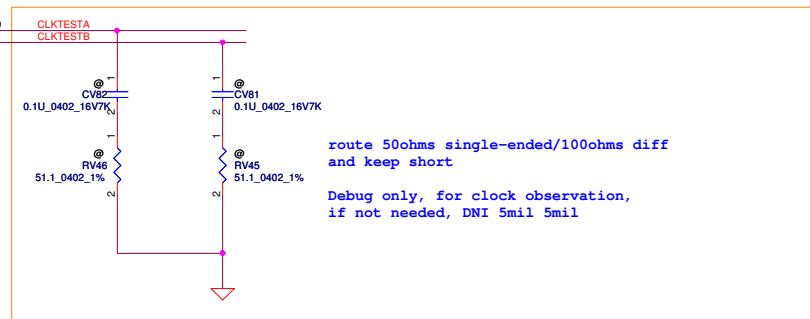
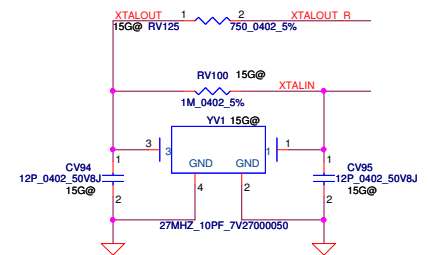
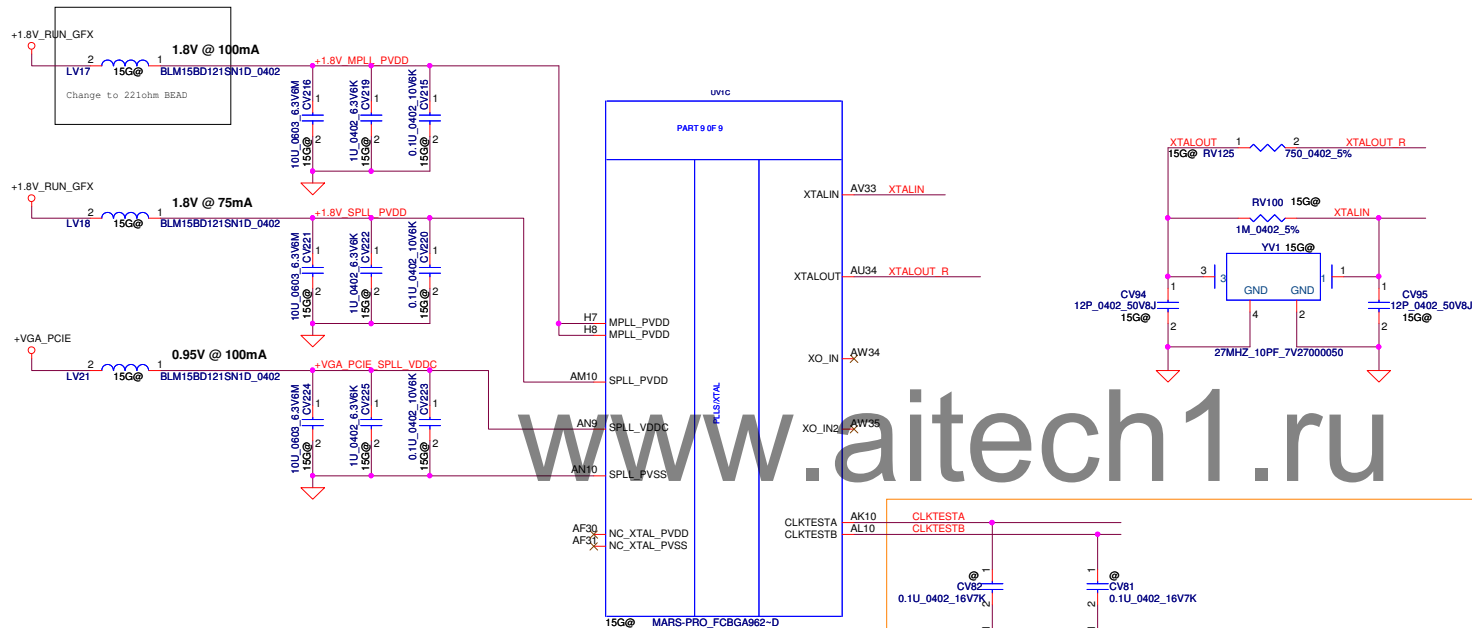


MLFS Bit	AMD recommended setting			
	strap	R_FU	R_PD	C
PS0:	11001	RV243=8.45K	RV201=2K	CV335=NC
PS1:	11000	RV237=NC	RV238=4.75K	CV329=NC
PS2:	00000	RV239=NC	RV240=4.75K	CV331=0.68u
PS3:	11000	RV241=NC	RV242=4.75K	CV333=NC

Date: Wednesday, April 10, 2013 Sheet 52 of 77



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MARX-PLL Power

Document Number

LA-9411P

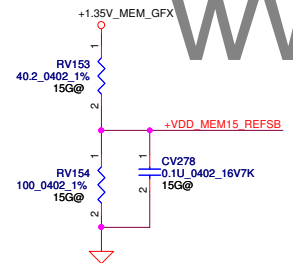
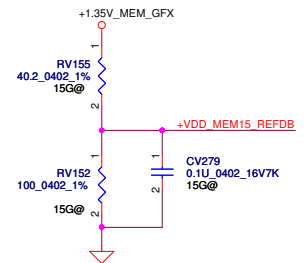
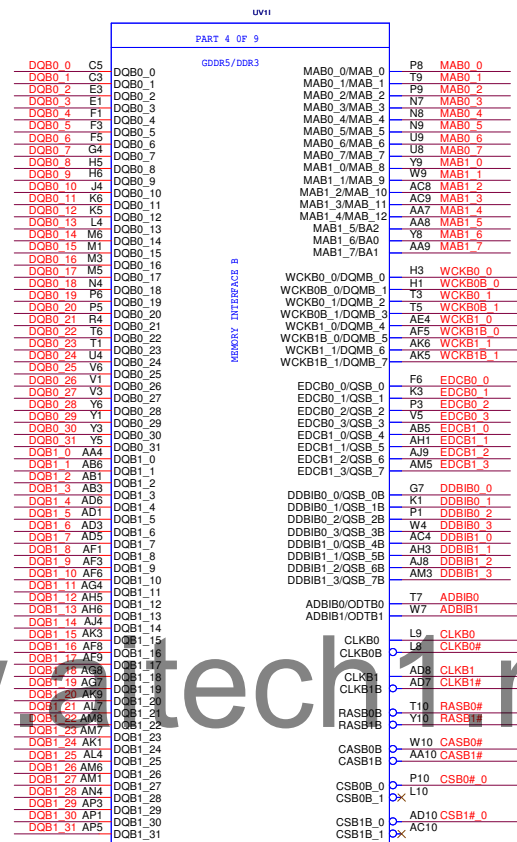
Date: Wednesday, April 10, 2013 Sheet 53 of 77 Rev 1.0

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GDDR5 CMD Mapping Table

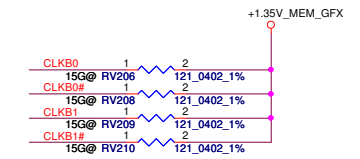
MARX MEM INTERFACE A		
PART 3 OF 9		
GDDR5/DMA3		
DDA0 [0..31]	<<>> DDA0 [0..31]	<56>
DDA1 [0..31]	<<>> DDA1 [0..31]	<57>
MAA0 [0..8]	<<>> MAA0 [0..8]	<56>
MAA1 [0..8]	<<>> MAA1 [0..8]	<57>
EDCA0 [0..3]	<<>> EDCA0 [0..3]	<56>
EDCA1 [0..3]	<<>> EDCA1 [0..3]	<57>
DDBA0 [0..3]	<<>> DDBA0 [0..3]	<56>
DDBA1 [0..3]	<<>> DDBA1 [0..3]	<57>
DDA0_0	C37	DDA0_0
DDA0_1	C38	DDA0_1
DDA0_2	A35	DDA0_2
DDA0_3	E34	DDA0_3
DDA0_4	C33	DDA0_4
DDA0_5	D33	DDA0_5
DDA0_6	F32	DDA0_6
DDA0_7	E32	DDA0_7
DDA0_8	D31	DDA0_8
DDA0_9	F30	DDA0_9
DDA0_10	C30	DDA0_10
DDA0_11	A30	DDA0_11
DDA0_12	F28	DDA0_12
DDA0_13	C28	DDA0_13
DDA0_14	A28	DDA0_14
DDA0_15	E28	DDA0_15
DDA0_16	D27	DDA0_16
DDA0_17	F26	DDA0_17
DDA0_18	C26	DDA0_18
DDA0_19	A26	DDA0_19
DDA0_20	F24	DDA0_20
DDA0_21	C24	DDA0_21
DDA0_22	A24	DDA0_22
DDA0_23	E24	DDA0_23
DDA0_24	D23	DDA0_24
DDA0_25	F22	DDA0_25
DDA0_26	C22	DDA0_26
DDA0_27	A22	DDA0_27
DDA0_28	F20	DDA0_28
DDA0_29	C20	DDA0_29
DDA0_30	A20	DDA0_30
DDA0_31	E19	DDA0_31
DDA0_32	D18	DDA0_32
DDA0_33	F17	DDA0_33
DDA0_34	C17	DDA0_34
DDA0_35	A17	DDA0_35
DDA0_36	F16	DDA0_36
DDA0_37	C16	DDA0_37
DDA0_38	A16	DDA0_38
DDA0_39	F15	DDA0_39
DDA0_40	C15	DDA0_40
DDA0_41	A15	DDA0_41
DDA0_42	F14	DDA0_42
DDA0_43	C14	DDA0_43
DDA0_44	A14	DDA0_44
DDA0_45	F13	DDA0_45
DDA0_46	C13	DDA0_46
DDA0_47	A13	DDA0_47
DDA0_48	F12	DDA0_48
DDA0_49	C12	DDA0_49
DDA0_50	A12	DDA0_50
DDA0_51	F11	DDA0_51
DDA0_52	C11	DDA0_52
DDA0_53	A11	DDA0_53
DDA0_54	F10	DDA0_54
DDA0_55	C10	DDA0_55
DDA0_56	A10	DDA0_56
DDA0_57	F09	DDA0_57
DDA0_58	C09	DDA0_58
DDA0_59	A09	DDA0_59
DDA0_60	F08	DDA0_60
DDA0_61	C08	DDA0_61
DDA0_62	A08	DDA0_62
DDA0_63	F07	DDA0_63
DDA0_64	C07	DDA0_64
DDA0_65	A07	DDA0_65
DDA0_66	F06	DDA0_66
DDA0_67	C06	DDA0_67
DDA0_68	A06	DDA0_68
DDA0_69	F05	DDA0_69
DDA0_70	C05	DDA0_70
DDA0_71	A05	DDA0_71
DDA0_72	F04	DDA0_72
DDA0_73	C04	DDA0_73
DDA0_74	A04	DDA0_74
DDA0_75	F03	DDA0_75
DDA0_76	C03	DDA0_76
DDA0_77	A03	DDA0_77
DDA0_78	F02	DDA0_78
DDA0_79	C02	DDA0_79
DDA0_80	A02	DDA0_80
DDA0_81	F01	DDA0_81
DDA0_82	C01	DDA0_82
DDA0_83	A01	DDA0_83
DDA0_84	F00	DDA0_84
DDA0_85	C00	DDA0_85
DDA0_86	A00	DDA0_86
DDA0_87	F00	DDA0_87
DDA0_88	C00	DDA0_88
DDA0_89	A00	DDA0_89
DDA0_90	F00	DDA0_90
DDA0_91	C00	DDA0_91
DDA0_92	A00	DDA0_92
DDA0_93	F00	DDA0_93
DDA0_94	C00	DDA0_94
DDA0_95	A00	DDA0_95
DDA0_96	F00	DDA0_96
DDA0_97	C00	DDA0_97
DDA0_98	A00	DDA0_98
DDA0_99	F00	DDA0_99
DDA0_100	C00	DDA0_100
DDA0_101	A00	DDA0_101
DDA0_102	F00	DDA0_102
DDA0_103	C00	DDA0_103
DDA0_104	A00	DDA0_104
DDA0_105	F00	DDA0_105
DDA0_106	C00	DDA0_106
DDA0_107	A00	DDA0_107
DDA0_108	F00	DDA0_108
DDA0_109	C00	DDA0_109
DDA0_110	A00	DDA0_110
DDA0_111	F00	DDA0_111
DDA0_112	C00	DDA0_112
DDA0_113	A00	DDA0_113
DDA0_114	F00	DDA0_114
DDA0_115	C00	DDA0_115
DDA0_116	A00	DDA0_116
DDA0_117	F00	DDA0_117
DDA0_118	C00	DDA0_118
DDA0_119	A00	DDA0_119
DDA0_120	F00	DDA0_120
DDA0_121	C00	DDA0_121
DDA0_122	A00	DDA0_122
DDA0_123	F00	DDA0_123
DDA0_124	C00	DDA0_124
DDA0_125	A00	DDA0_125
DDA0_126	F00	DDA0_126
DDA0_127	C00	DDA0_127
DDA0_128	A00	DDA0_128
DDA0_129	F00	DDA0_129
DDA0_130	C00	DDA0_130
DDA0_131	A00	DDA0_131
DDA0_132	F00	DDA0_132
DDA0_133	C00	DDA0_133
DDA0_134	A00	DDA0_134
DDA0_135	F00	DDA0_135
DDA0_136	C00	DDA0_136
DDA0_137	A00	DDA0_137
DDA0_138	F00	DDA0_138
DDA0_139	C00	DDA0_139
DDA0_140	A00	DDA0_140
DDA0_141	F00	DDA0_141
DDA0_142	C00	DDA0_142
DDA0_143	A00	DDA0_143
DDA0_144	F00	DDA0_144
DDA0_145	C00	DDA0_145
DDA0_146	A00	DDA0_146
DDA0_147	F00	DDA0_147
DDA0_148	C00	DDA0_148
DDA0_149	A00	DDA0_149
DDA0_150	F00	DDA0_150
DDA0_151	C00	DDA0_151
DDA0_152	A00	DDA0_152
DDA0_153	F00	DDA0_153
DDA0_154	C00	DDA0_154
DDA0_155	A00	DDA0_155
DDA0_156	F00	DDA0_156
DDA0_157	C00	DDA0_157
DDA0_158	A00	DDA0_158
DDA0_159	F00	DDA0_159
DDA0_160	C00	DDA0_160
DDA0_161	A00	DDA0_161
DDA0_162	F00	DDA0_162
DDA0_163	C00	DDA0_163
DDA0_164	A00	DDA0_164
DDA0_165	F00	DDA0_165
DDA0_166	C00	DDA0_166
DDA0_167	A00	DDA0_167
DDA0_168	F00	DDA0_168
DDA0_169	C00	DDA0_169
DDA0_170	A00	DDA0_170
DDA0_171	F00	DDA0_171
DDA0_172	C00	DDA0_172
DDA0_173	A00	DDA0_173
DDA0_174	F00	DDA0_174
DDA0_175	C00	DDA0_175
DDA0_176	A00	DDA0_176
DDA0_177	F00	DDA0_177
DDA0_178	C00	DDA0_178
DDA0_179	A00	DDA0_179
DDA0_180	F00	DDA0_180
DDA0_181	C00	DDA0_181
DDA0_182	A00	DDA0_182
DDA0_183	F00	DDA0_183
DDA0_184	C00	DDA0_184
DDA0_185	A00	DDA0_185
DDA0_186	F00	DDA0_186
DDA0_187	C00	DDA0_187
DDA0_188	A00	DDA0_188
DDA0_189	F00	DDA0_189
DDA0_190	C00	DDA0_190
DDA0_191	A00	DDA0_191
DDA0_192	F00	DDA0_192
DDA0_193	C00	DDA0_193
DDA0_194	A00	DDA0_194
DDA0_195	F00	DDA0_195
DDA0_196	C00	DDA0_196
DDA0_197	A00	DDA0_197
DDA0_198	F00	DDA0_198
DDA0_199	C00	DDA0_199
DDA0_200	A00	DDA0_200
DDA0_201	F00	DDA0_201
DDA0_202	C00	DDA0_202
DDA0_203	A00	DDA0_203
DDA0_204	F00	DDA0_204
DDA0_205	C00	DDA0_205
DDA0_206	A00	DDA0_206
DDA0_207	F00	DDA0_207
DDA0_208	C00	DDA0_208
DDA0_209	A00	DDA0_209
DDA0_210	F00	DDA0_210
DDA0_211	C00	DDA0_211
DDA0_212	A00	DDA0_212
DDA0_213	F00	DDA0_213
DDA0_214	C00	DDA0_214
DDA0_215	A00	DDA0_215
DDA0_216	F00	DDA0_216
DDA0_217	C00	DDA0_217
DDA0_218	A00	DDA0_218
DDA0_219	F00	DDA0_219
DDA0_220	C00	DDA0_220
DDA0_221	A00	DDA0_221
DDA0_222	F00	DDA0_222
DDA0_223	C00	DDA0_223
DDA0_224	A00	DDA0_224
DDA0_225	F00	DDA0_225
DDA0_226	C00	DDA0_226
DDA0_227	A00	DDA0_227
DDA0_228	F00	DDA0_228
DDA0_229	C00	DDA0_229
DDA0_230	A00	DDA0_230
DDA0_231	F00	DDA0_231
DDA0_232	C00	DDA0_232
DDA0_233	A00	DDA0_233
DDA0_234	F00	DDA0_234
DDA0_235	C00	DDA0_235
DDA0_236	A00	DDA0_236
DDA0_237	F00	DDA0_237
DDA0_238	C00	DDA0_238
DDA0_239	A00	DDA0_239
DDA0_240	F00	DDA0_240
DDA0_241	C00	DDA0_241
DDA0_242	A00	DDA0_242
DDA0_243	F00	DDA0_243
DDA0_244	C00	DDA0_244
DDA0_245	A00	DDA0_245
DDA0_246	F00	DDA0_246
DDA0_247	C00	DDA0_247
DDA0_248	A00	DDA0_248
DDA0_249	F00	DDA0_249
DDA0_250	C00	DDA0_250
DDA0_251	A00	DDA0_251
DDA0_252	F00	DDA0_252
DDA0_253	C00	DDA0_253
DDA0_254	A00	DDA0_254
DDA0_255	F00	DDA0_255
DDA0_256	C00	DDA0_256
DDA0_257	A00	DDA0_257
DDA0_258	F00	DDA0_258
DDA0_259	C00	DDA0_259
DDA0_260	A00	DDA0_260
DDA0_261	F00	DDA0_261
DDA0_262	C00	DDA0_262
DDA0_263	A00	DDA0_263
DDA0_264	F00	DDA0_264
DDA0_265	C00	DDA0_265
DDA0_266	A00	DDA0_266
DDA0_267	F00	DDA0_267
DDA0_268	C00	DDA0_268
DDA0_269	A00	DDA0_269
DDA0_270	F00	DDA0_270
DDA0_271	C00	DDA0_271
DDA0_272	A00	DDA0_272
DDA0_273	F00	DDA0_273
DDA0_274	C00	DDA0_274
DDA0_275	A00	DDA0_275
DDA0_276	F00	DDA0_276
DDA0_277	C00	DDA0_277
DDA0_278	A00	DDA0_278
DDA0_279	F00	DDA0_279
DDA0_280	C00	DDA0_280
DDA0_281	A00	DDA0_281
DDA0_282	F00	DDA0_282
DDA0_283	C00	DDA0_283
DDA0_284	A00	DDA0_284
DDA0_285	F00	DDA0_285
DDA0_286	C00	DDA0_286
DDA0_287	A00	DDA0_287
DDA0_288	F00	DDA0_288
DDA0_289	C00	DDA0_289
DDA0_290	A00	DDA0_290
DDA0_291	F00	DDA0_291
DDA0_292	C00	DDA0_292
DDA0_293	A00	DDA0_293
DDA0_294	F00	DDA0_294
DDA0_295	C00	DDA0_295
DDA0_296	A00	DDA0_296
DDA0_297	F00	DDA0_297
DDA0_298	C00	DDA0_298
DDA0_299	A00	DDA0_299
DDA0_300	F00	DDA0_300
DDA0_301	C00	DDA0_301
DDA0_302	A00	DDA0_302
DDA0_303	F00	DDA0_303
DDA0_304	C00	DDA0_304
DDA0_305	A00	DDA0_305
DDA0_306	F00	DDA0_306
DDA0_307	C00	DDA0_307
DDA0_308	A00	DDA0_308
DDA0_309	F00	DDA0_309
DDA0_310	C00	DDA0_310
DDA0_311	A00	DDA0_311
DDA0_312	F00	DDA0_312
DDA0_313	C00	DDA0_313
DDA0_314	A00	DDA0_314
DDA0_315	F00	DDA0_315
DDA0_316	C00	DDA0_316
DDA0_317	A00	DDA0_317
DDA0_318	F00	DDA0_318
DDA0_319	C00	DDA0_319
DDA0_320	A00	DDA0_320
DDA0_321	F00	DDA0_321
DDA0_322	C00	DDA0_322
DDA0_323	A00	DDA0_323
DDA0_324	F00</	

DOB0 [0..31] << >> DOB0 [0..31] <58>
DOB1 [0..31] << >> DOB1 [0..31] <59>
MAB0 [0..8] << >> MAB0 [0..8] <58>
MAB1 [0..8] << >> MAB1 [0..8] <59>
EDCB0 [0..3] << >> EDCB0 [0..3] <58>
EDCB1 [0..3] << >> EDCB1 [0..3] <59>
DDBIB0 [0..3] << >> DDBIB0 [0..3] <58>
DDBIB1 [0..3] << >> DDBIB1 [0..3] <59>



+VDD_MEM15_REFDB Y12
-VDD_MEM15_REFSB AA12

MVREFDB
MVREFSB



This basic topology should be used for DRAM_RST for DDR3/GDDR5. These Capacitors and Resistor values are an example only. The Series R and | | Cap values will depend on the DRAM load and will have to be calculated for different Memory ,DRAM Load and board to pass Reset Signal Spec.
Place all these components very close to GPU (Within 25mm) and keep all component close to each Other (within 5mm) except Rser2

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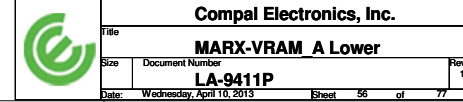


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Title		
MARX-MEM Interface B		
Size	Document Number	Rev
	LA-9411P	1.0
Date:	Wednesday, April 10, 2013	Sheet 55 of 77

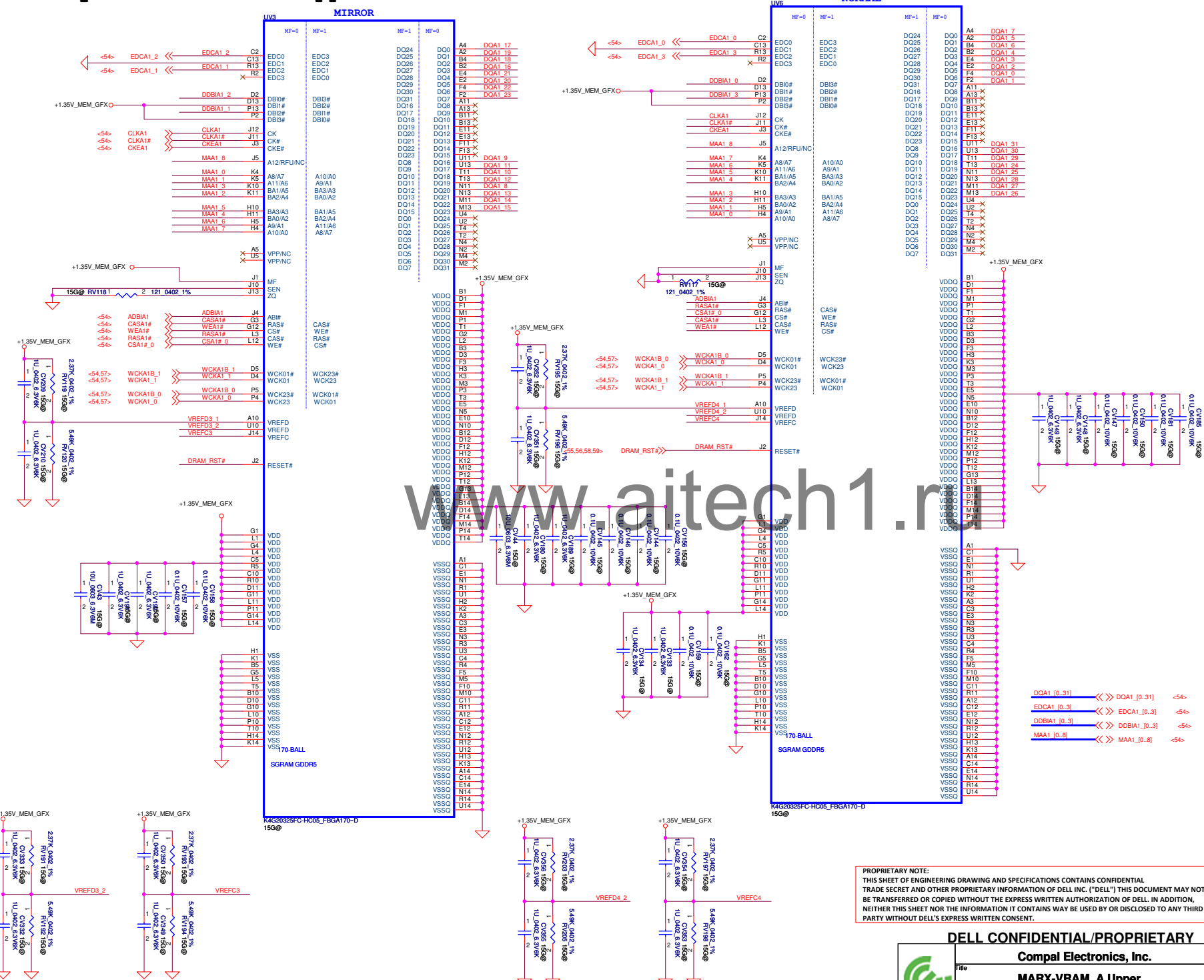
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2

MIRROR



Memory Partition A - Upper 16 bits



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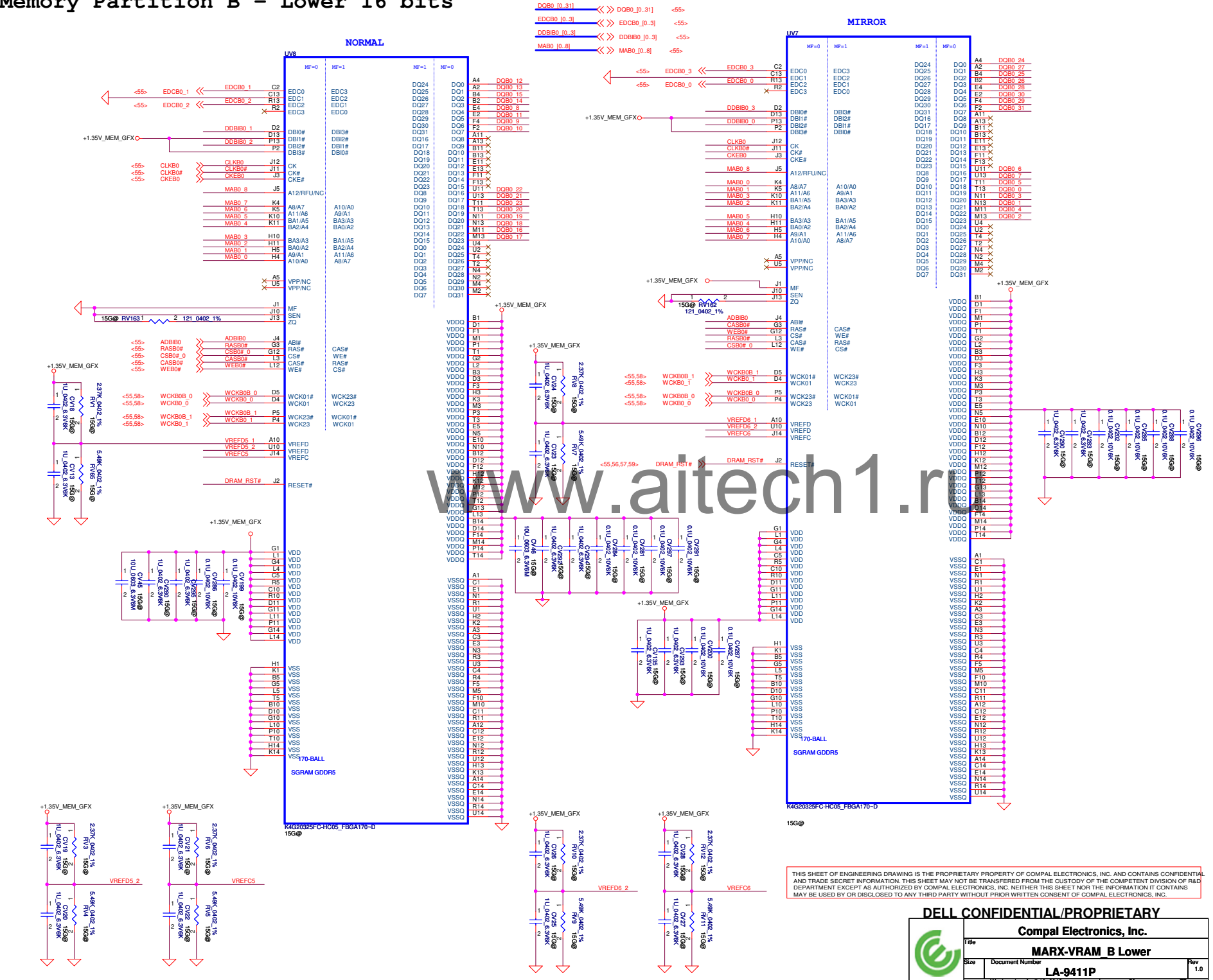
MARX-VRAM A Upper

LA-9411P

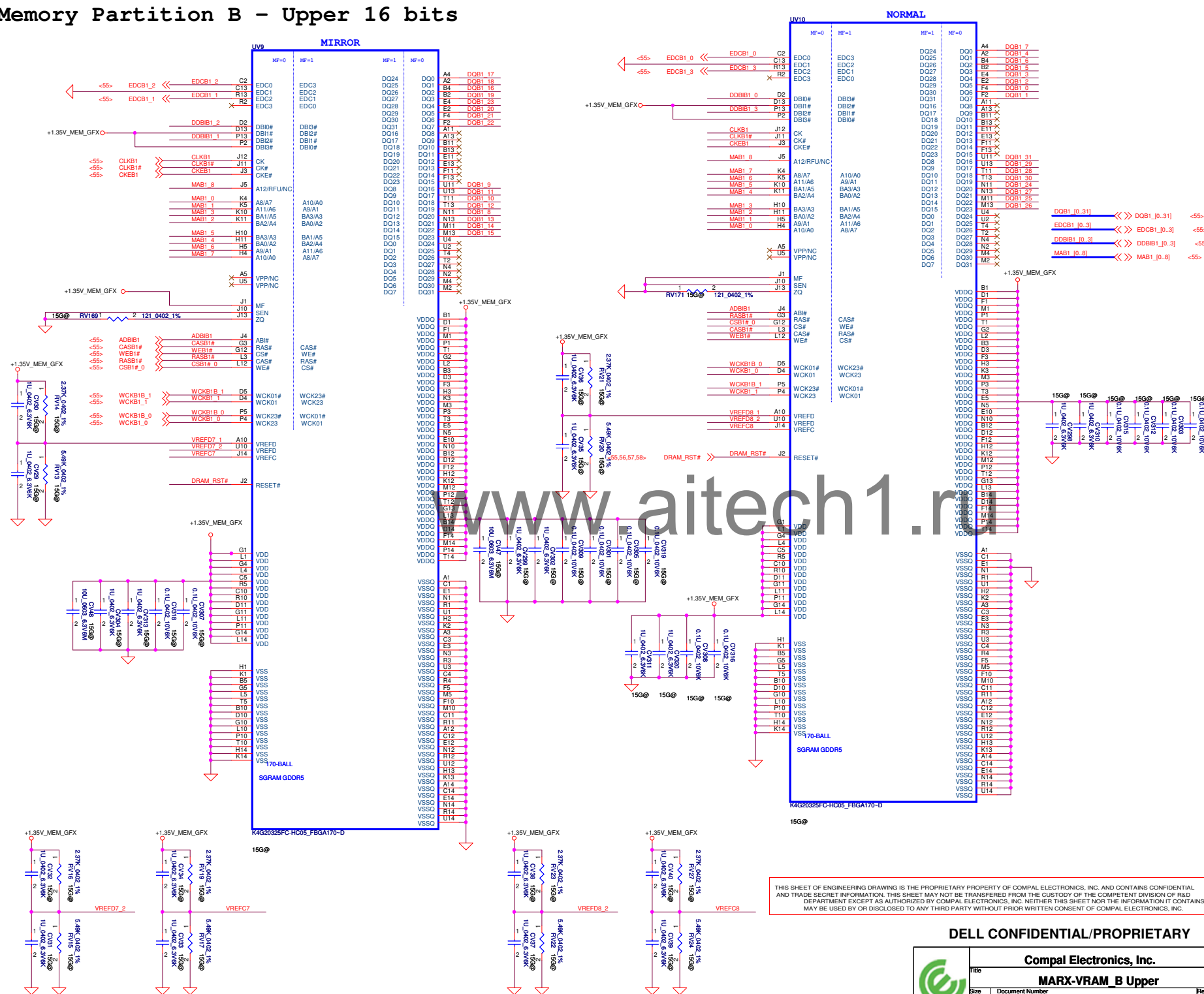
Rev
1.0

Date: Wednesday, April 10, 2013 Sheet 57 of 77

Memory Partition B - Lower 16 bits




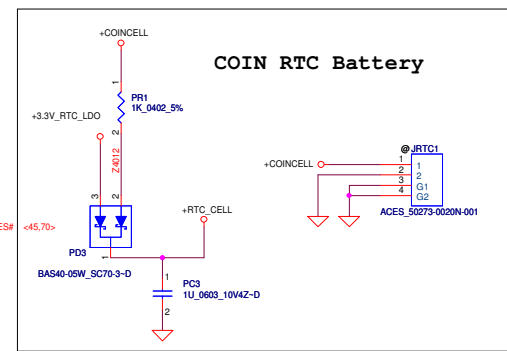
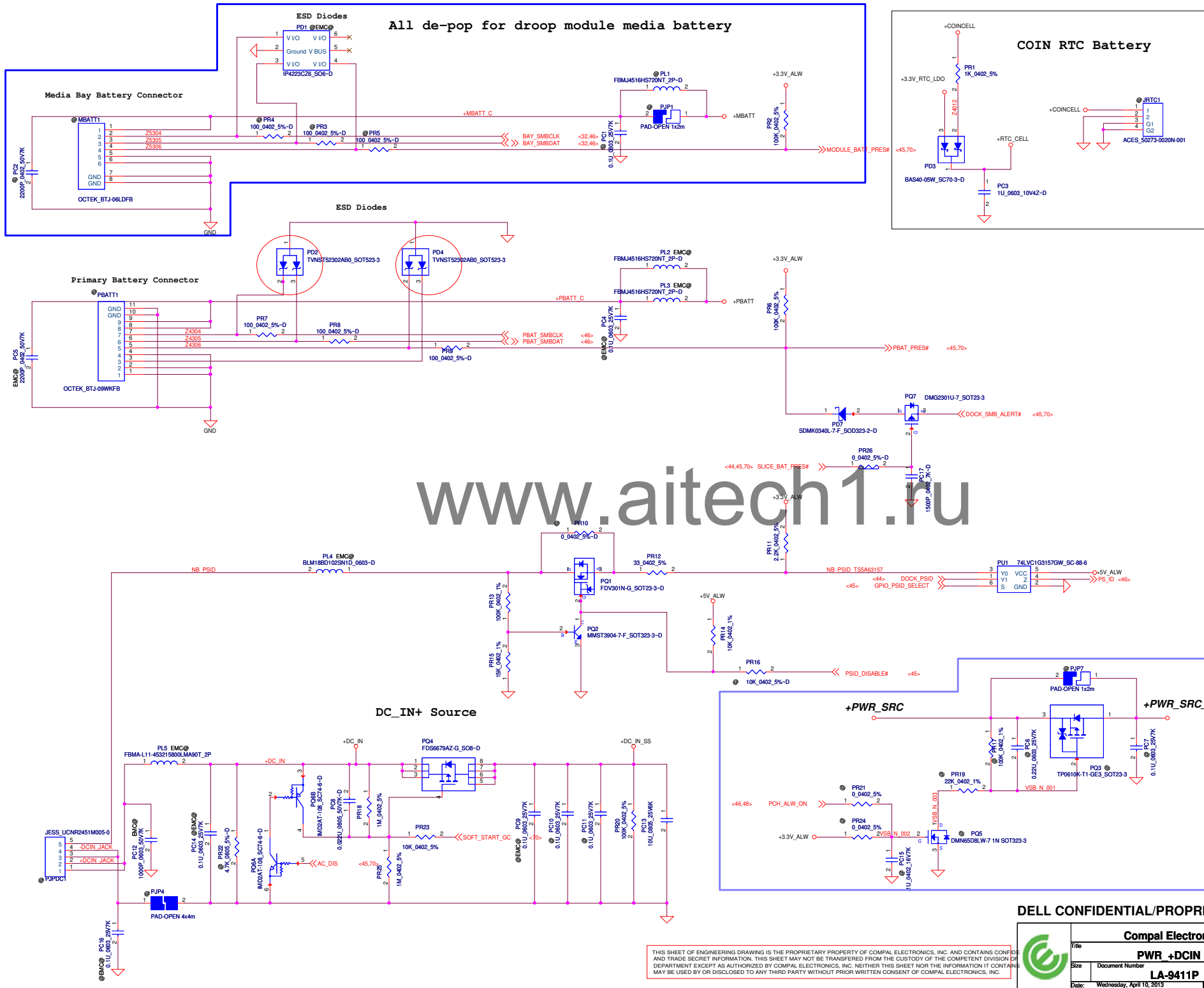
Memory Partition B - Upper 16 bits



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	Title			
	MARX-VRAM B Upper			
	Size	Document Number		Rev
	LA-9411P		1.0	
Date:	Wednesday, April 10, 2013		Sheet 59 of 77	



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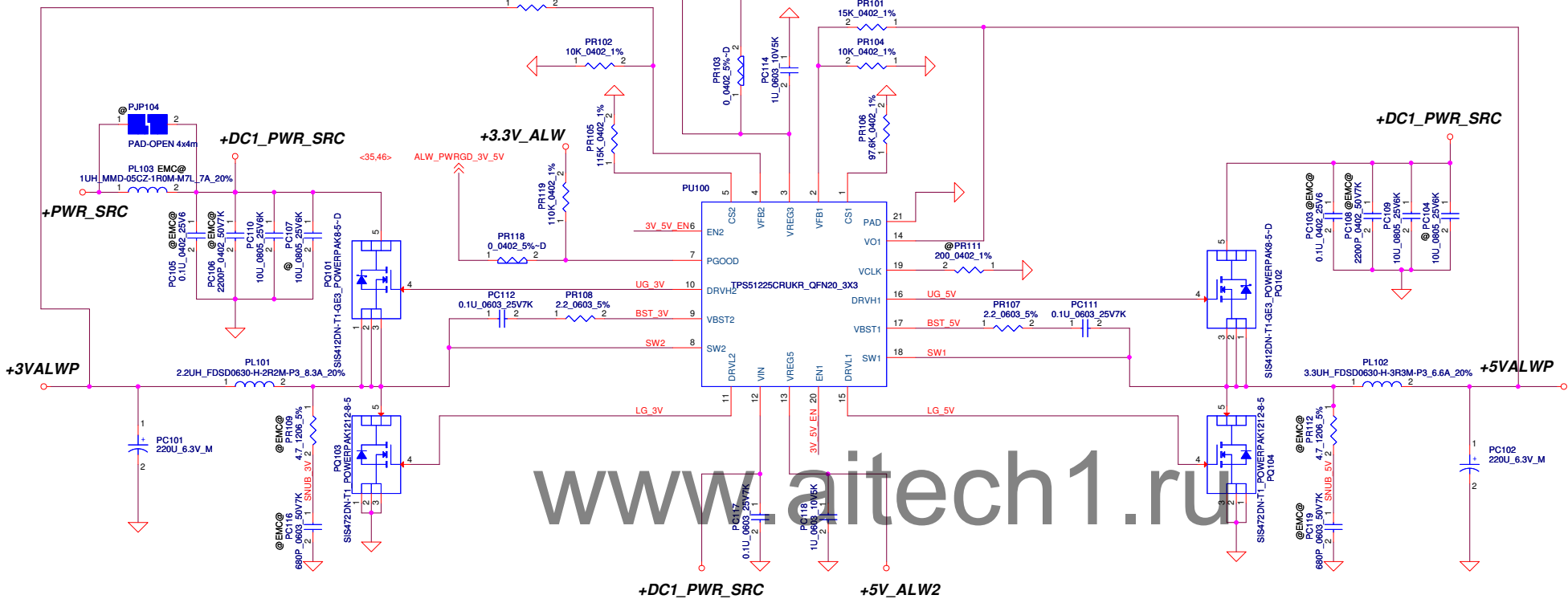
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$$VFB2=2V, PR100=(V_{out}-0.5 \cdot V_{ripple}-2)/2 \cdot PR102$$

+3.3V_ALW2

+3.3V_RTC_LDO

$$VFB1=2V, PR101=(V_{out}-0.5 \cdot V_{ripple}-2)/2 \cdot PR104$$

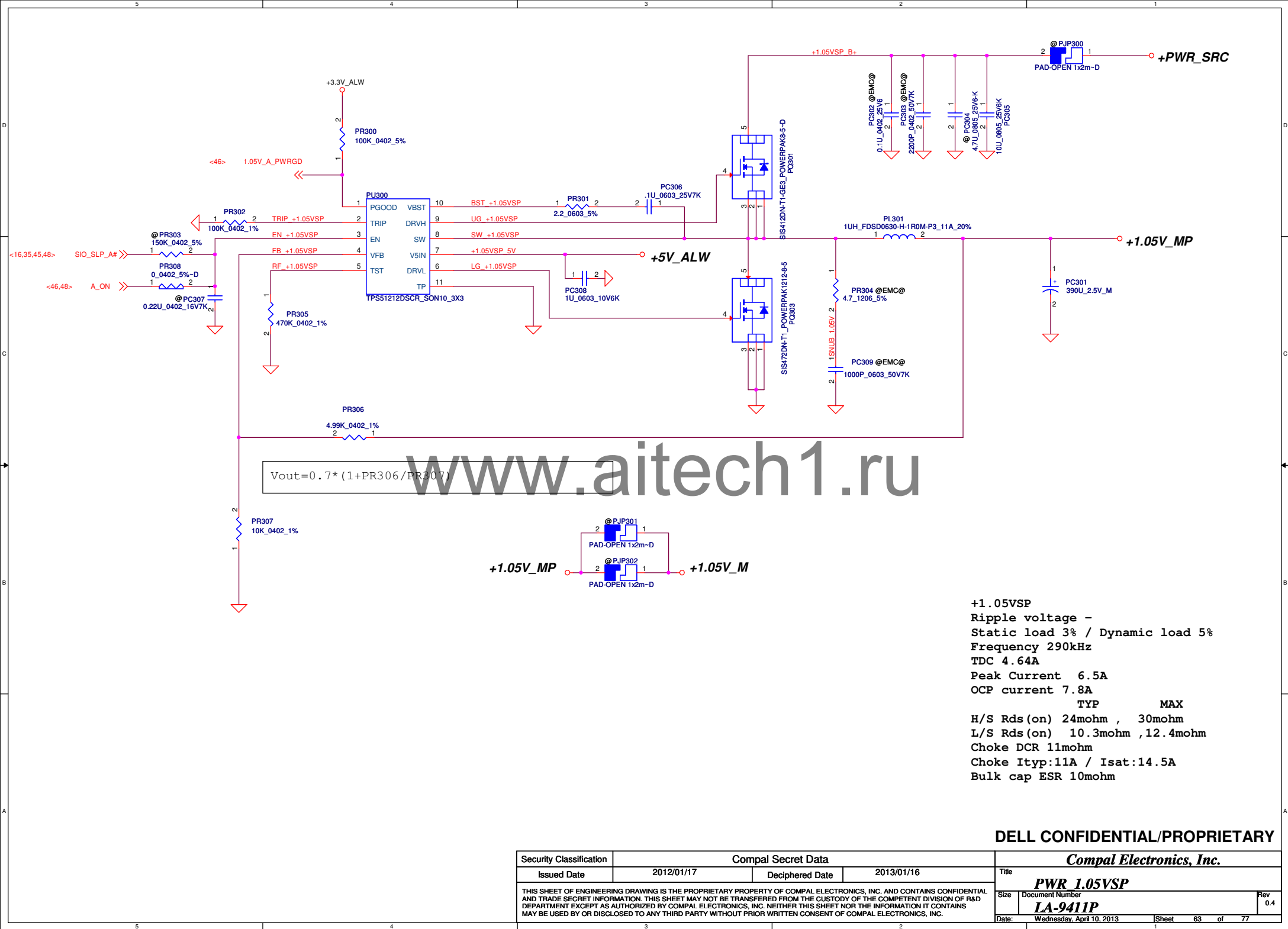


3VALWP
 Ripple voltage -
 Static load 3% / Dynamic load 5%
 Frequency 350kHz
 TDC 7.33A
 Peak Current 10.48A
 OCP current 12.57A
 TYP MAX
 H/S Rds(on) 24mohm , 30mohm
 L/S Rds(on) 10.3mohm , 12.4mohm
 Choke DCR Max:17mohm
 Choke Ityp:8.3A / Isat:10.8A
 Bulk cap ESR 15mohm

5VALWP
 Ripple voltage -
 Static load 3% / Dynamic load 5%
 Frequency 300kHz
 TDC 5.613A
 Peak Current 8A
 OCP current 9.6A
 TYP MAX
 H/S Rds(on) 24mohm , 30mohm
 L/S Rds(on) 10.3mohm , 12.4mohm
 Choke DCR Max:28mohm
 Choke Ityp:6.6A / Isat:8.2A
 Bulk cap ESR 15mohm

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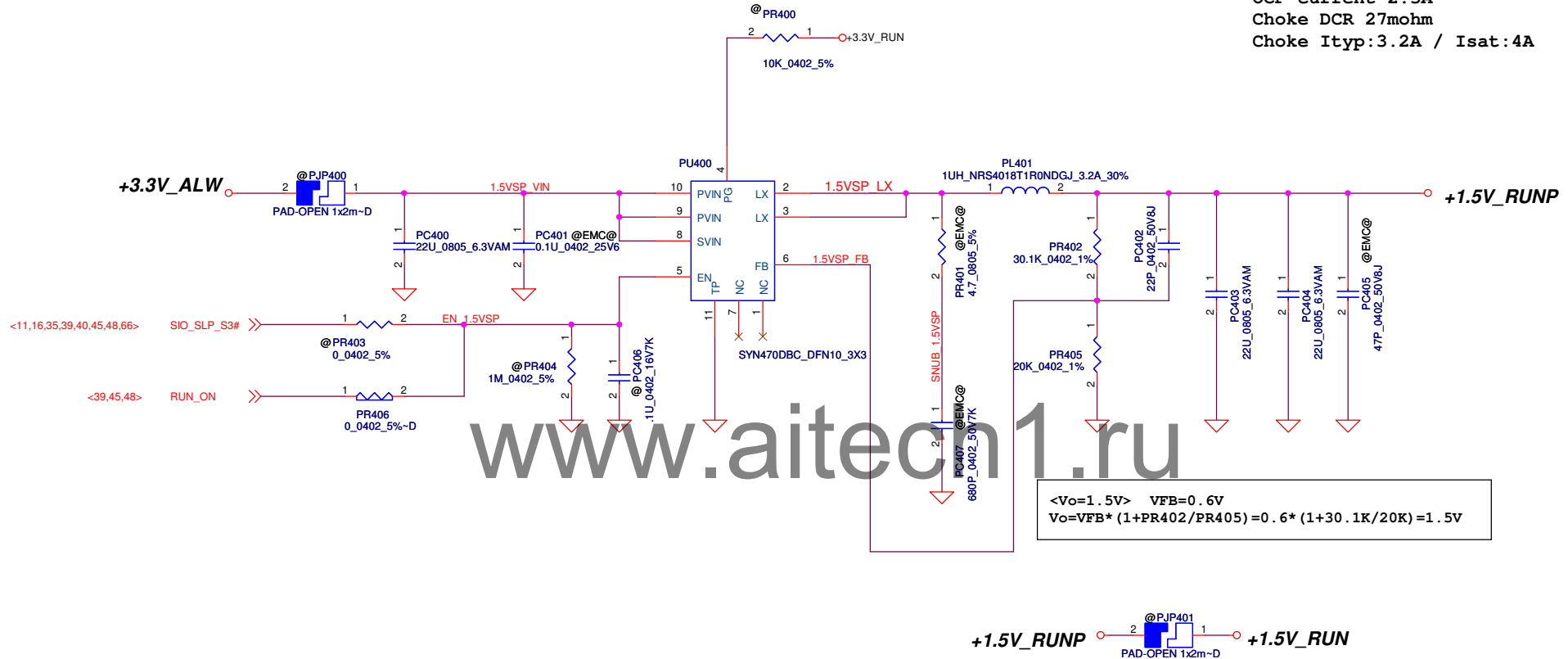
Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2012/01/17	Deciphered Date	2013/01/16	Title	PWR 3VALWP/5VALWP
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				Date	Wednesday, April 10, 2013
				Sheet	61 of 77



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Security Classification		Compal Secret Data		Title	
Issued Date	2012/01/17	Deciphered Date	2013/01/16	PWR 1.05VSP	
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				LA-9411P	Rev 0.4
				Date	Wednesday, April 10, 2013
				Sheet	63 of 77

+1.5VSP
Ripple voltage -
Static load 3% / Dynamic load 5%
Frequency 1MHz
TDC 1.329A
Peak Current 1.9A
OCP current 2.3A
Choke DCR 27mohm
Choke I_{typ}:3.2A / I_{sat}:4A



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Title

PWR_+1.5VSP

Size

Document Number

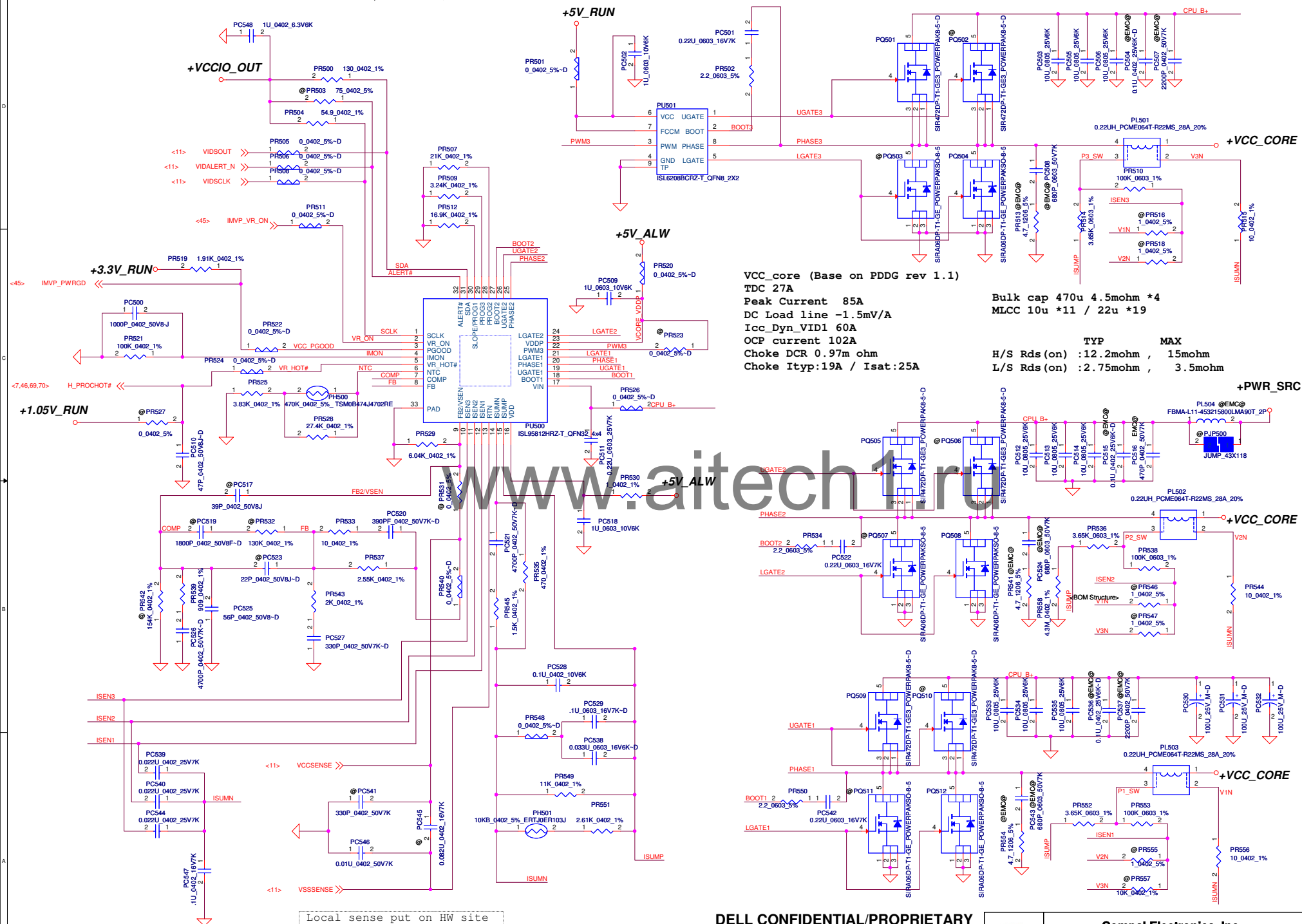
LA-9411P

Date _____

Wednesday, April 10, 2013

Sheet 64 of 77

Rev
0.4



VCC_core (Base on PDDG rev 1.1)
TDC 27A
Peak Current 85A
DC Load line -1.5mV/A
Icc_Dyn_VID1 60A
OCP current 102A
Choke DCR 0.97m ohm
Choke Ityp:19A / Isat:25A

Bulk cap 470u 4.5mohm *4
MLCC 10u *11 / 22u *19

	TYP	MAX
H/S Rds(on)	:12.2mohm	15mohm
L/S Rds(on)	:2.75mohm	3.5mohm

Local sense put on HW site

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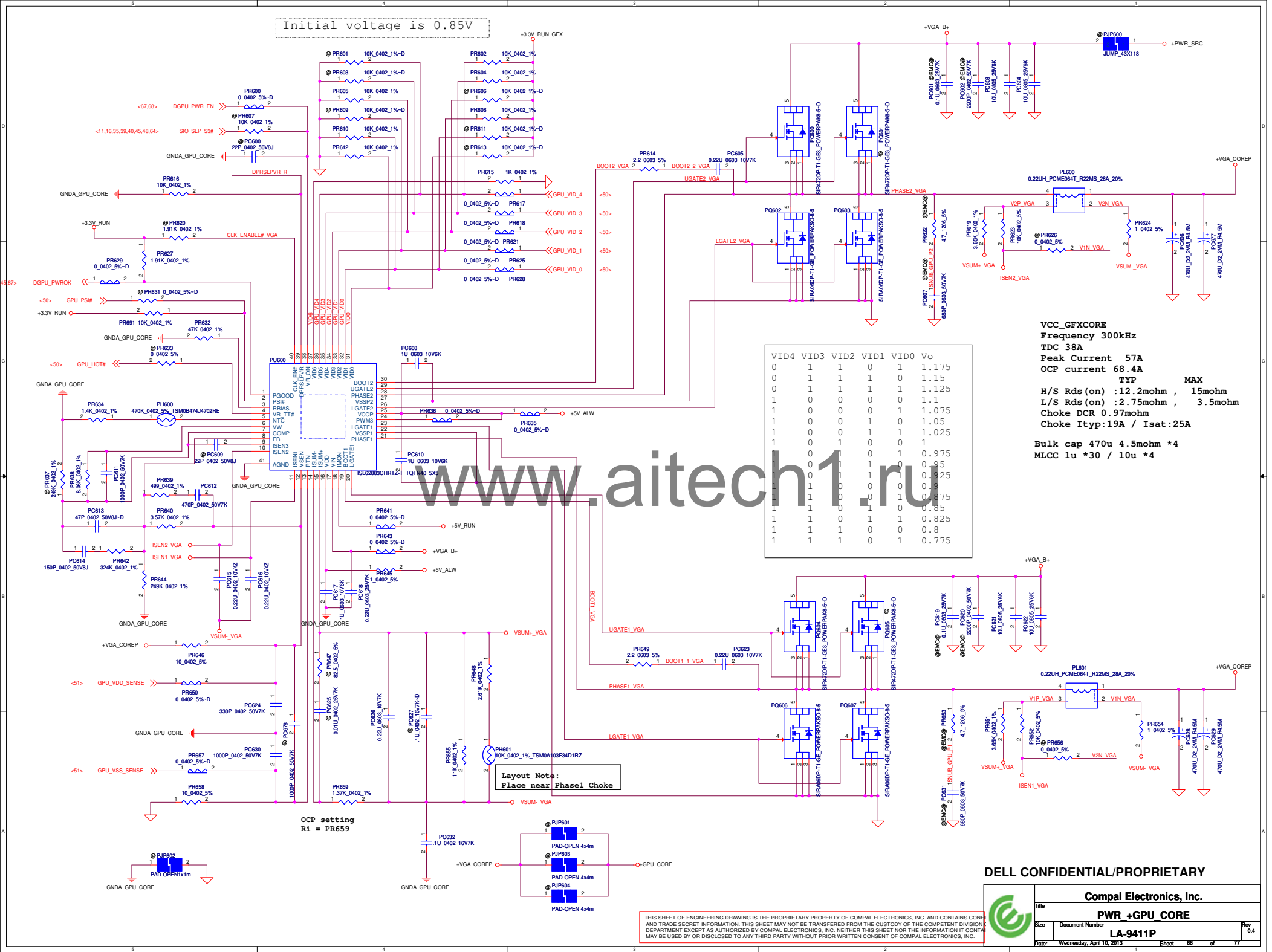
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PWR_VCORE_ISL95812 for QC

Size Document Number LA-9411P

Date: Wednesday, April 10, 2013 Sheet 85 of 77

Initial voltage is 0.85V



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PWR +GPU CORE			
Size	Document Number	Rev	
	LA-9411P	0.4	
Date	Wednesday, April 10, 2013	Sheet	66 of 77

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$$V_{FB}=0.6V \quad V_o=V_{FB} \cdot (1+PR683/PR684)=0.6 \cdot (1+5.9K/10K)=0.95V$$

+5V_ALW

<66,67>

+3.3V_RUN

+3.3V_ALW

<66,67>

$$V_{FB}=0.6V \quad V_o=V_{FB} \cdot (1+PR687/PR689)=0.6 \cdot (1+20K/10K)=1.8V$$

PCIE_VDDC_PWRGD 2 1 +3.3V_RUN

@PR679
10K_0402_5%

+VGA_PCIEP

+VGA_PCIEP (0.95V)

Ripple voltage -

Static load 3% / Dynamic load 5%

Frequency 1MHz

TDC 3.2A

Peak Current 4.56A

OCP current 5.47A

Choke DCR 29mohm

Choke Ityp:4.9A / Isat:9A

+VGA_PCIEP

1.8Volt

Ripple voltage -

Static load 3% / Dynamic load 5%

Frequency 1MHz

TDC 1.43A

Peak Current 2A

OCP current 2.46A

Choke DCR 27mohm

Choke Ityp:3.2A / Isat:4A

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Title **PWR +VGA_PCIEP/+1.8V_RUN GFX**

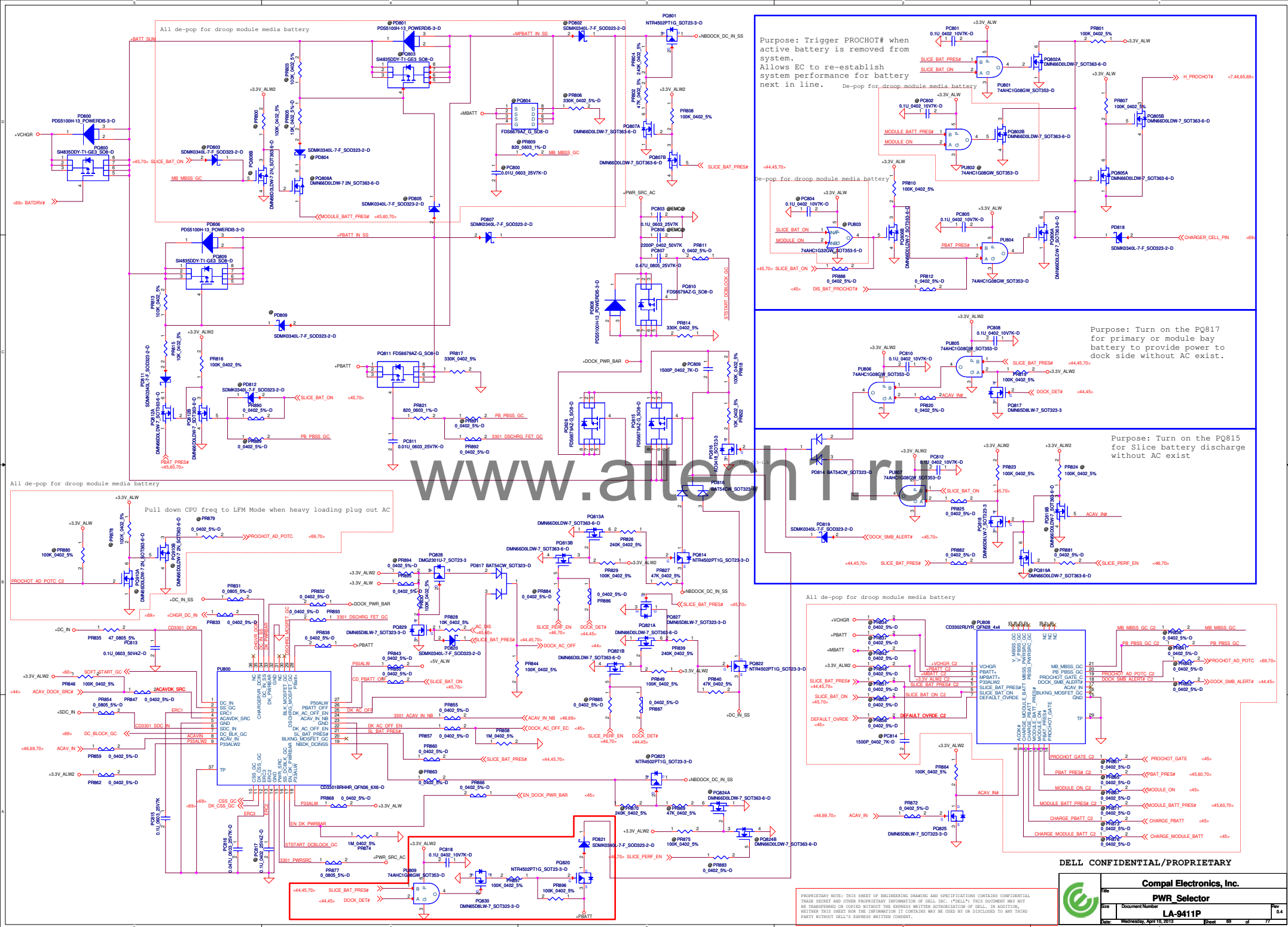
Size Document Number

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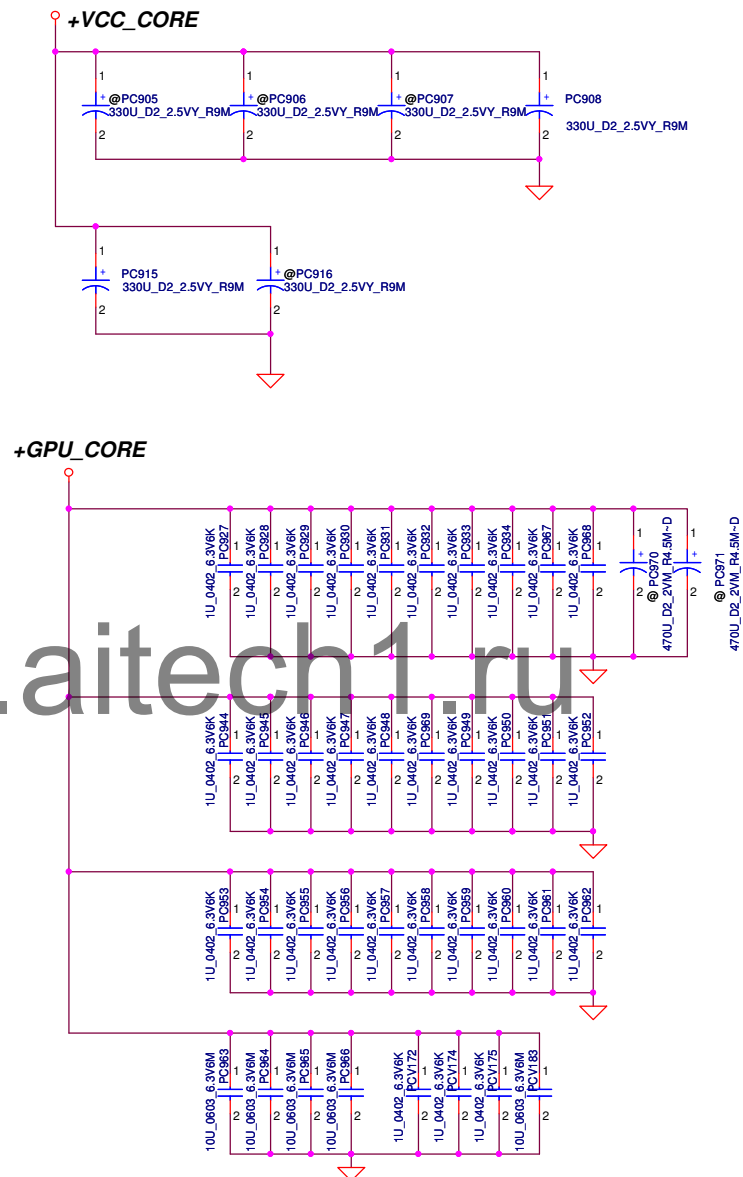
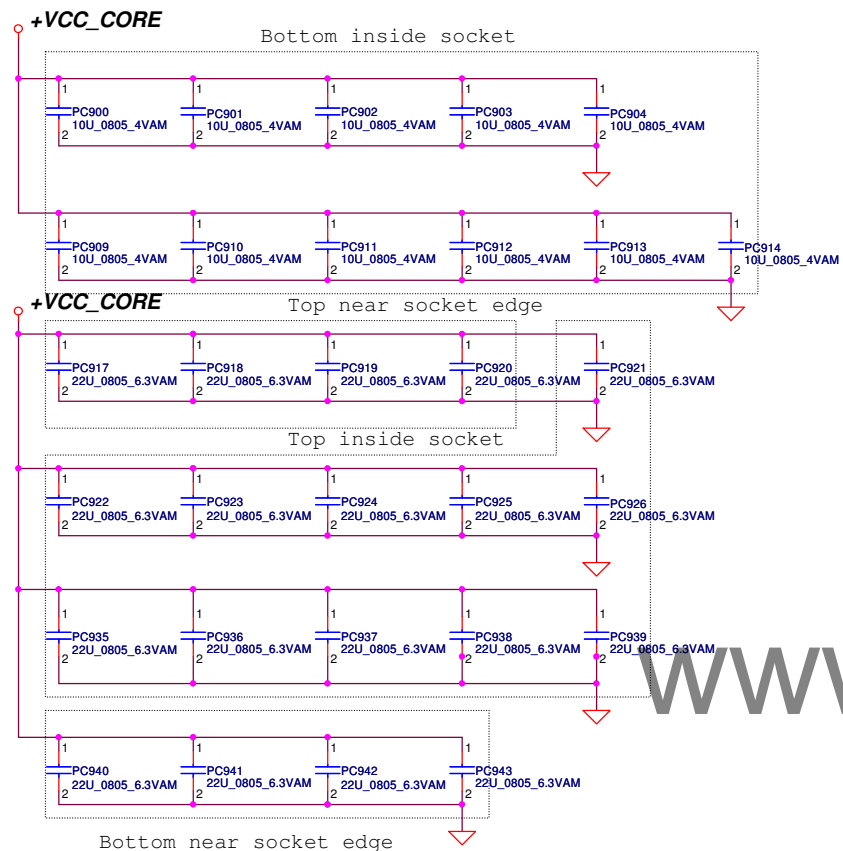
Rev
0.4

Date: Wednesday, April 10, 2013 Sheet 67 of 77

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Based on PDDG rev 1.1 Table 5-1.



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PWR PROCESSOR DECOUPLING

Size	Document Number
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LA-9411P

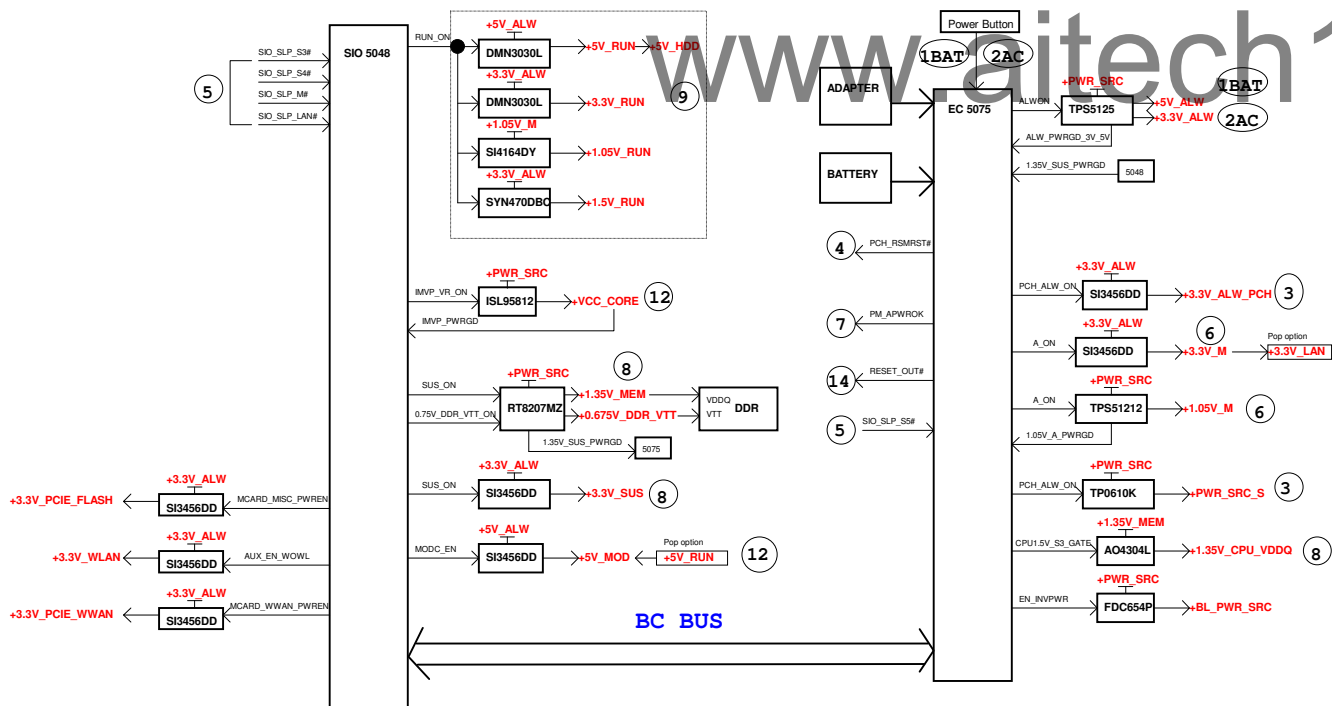
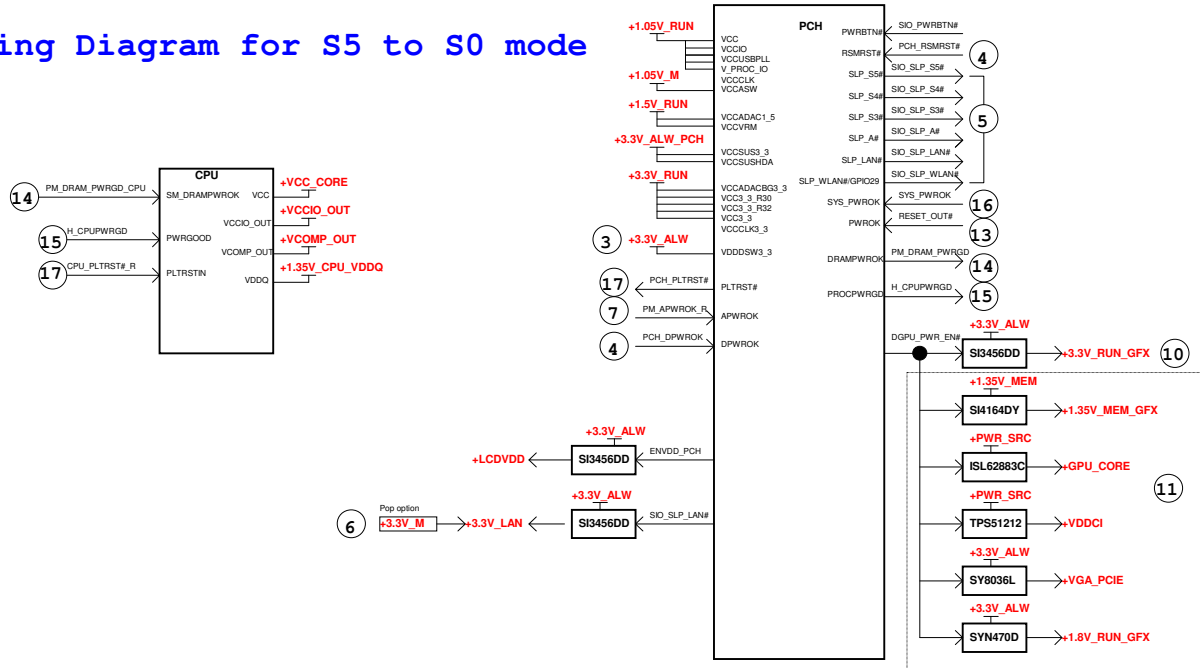
Rev	0.4
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Date: Wednesday, April 10, 2013

Sheet 70 of 77

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Timing Diagram for S5 to S0 mode



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Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	7	HW	8/24/2012	COMPAL	Change DRAMPWROK Pull up Power rail to Suspend	Base on EDS 1.0 (page124). Change RC4 PM_DRAM_PWRGD pull up power rail to +3.3V_ALW_PCH.	X00(0.2)
2	16	HW	8/24/2012	COMPAL	Remove DGPU_HOLD_RST# double pull up.	Remove RH74 DGPU_HOLD_RST# pull up.	X00(0.2)
3	20	HW	8/24/2012	COMPAL	Remove mCARD_PCIE_SATA# double pull up.	Remove RH196 mCARD_PCIE_SATA# pull up.	X00(0.2)
4	48	HW	8/27/2012	COMPAL	Correct DC to DC interface Pull up power rail to +PWR_SRC_S	R905.1, R911.1, R917.1, R930.1, R906.1 and R912.1 change to +PWR_SRC_S	X00(0.2)
5	13,14	HW	8/27/2012	COMPAL	Follow DG DDR3L VREF_DQ Control as page120. it pull up power rail should be +1.35V_MEM	Modify RD19.1, RD22.1, RD15.1 net name to +1.35V_MEM.	X00(0.2)
6	46,16	HW	8/30/2012	COMPAL	Follow EDS page 131 as DSW rail	Modify AC_PRESENT R835.1 to +PCH_VCCDSW3_3 Add PCH_PCIE_WAKE# RH92.1 to +PCH_VCCDSW3_3 De-populate RH78 with +3.3V_ALW_PCH power rail	X00(0.2)
7	46	HW	8/27/2012	COMPAL	Correct GPU_SMBDAT,GPU_SMBCLK Pull up power rail to +3.3V_RUN	Modify GPU_SMBDAT R829,1,GPU_SMBCLK R822.1 to +3.3V_RUN	X00(0.2)
8	33	HW	8/27/2012	COMPAL	Change LANWAKE#_R Pull up power rail to +3.3V_LAN	Modify R558.1 power rail to +3.3V_LAN	X00(0.2)
9	46	HW	8/29/2012	COMPAL	Modify THERMATRIP2# control by +VCCIO_OUT	Modify Q4.2 to +VCCIO_OUT.	X00(0.2)
10	47	HW	8/27/2012	COMPAL	Back E4 RSMRST RESET IC solution and add pull up at PCH_RSMRST#_Q	Modify U8 to RT9818A-44GU3 Add Pull up 8.2Kohm to +3.3V_ALW_PCH on PCH_RSMRST#_Q	X00(0.2)
11	35	HW	8/27/2012	COMPAL	Back E4 JUSH pin out	JUSH1 back to 20pins.	X00(0.2)
12	51	HW	8/27/2012	AMD	Modify GPU power net	+VDDCI change to +GPU_CORE power net	X00(0.2)
13	48	HW	8/27/2012	COMPAL	Correct +1.35V_CPU_VDDQ Discharge net name	Modify R926.2 Net name to +1.35V_CPU_VDDQ	X00(0.2)
14	36	HW	8/27/2012	COMPAL	Update OZ777 ES2 symbol	U38 OZ777FJ2LN_QFN48P_6X6 symbol updated	X00(0.2)
15	38	HW	8/27/2012	COMPAL	Replace U7 SATA Repeater and U95 SATA/PCIE SW by U7 ASM1467 SATA/PCIE Repeater.	Modify U7 circuit	X00(0.2)
16	33,34	HW	9/4/2012	COMPAL	LAN LED support unobtrusive mode on System board	Modify Q325,Q326 LAN LED control circuit between LAN SW MB and MB CONN.	X00(0.2)
17	16	HW	8/27/2012	COMPAL	Base on EDS 1.0 Page 124 Modify SIO_SLP_LAN# to DSW Power rail	Modify SIO_SLP_LAN# RH80.1 to +PCH_VCCDSW3_3	X00(0.2)
18	37	HW	8/27/2012	COMPAL	Modify CPPE#, USB_MCARD1_DET# Pull up power rail to +3.3V_RUN	Modify CPPE# R737.2, USB_MCARD1_DET# R739.2 net name to +3.3V_RUN	X00(0.2)
19	29	HW	8/28/2012	DELL	Cost Down Concept	Replace (U21,U24) NOT Gate by (Q5, Q6) N-Channel MOSFET with Pull high resistor on CA_DET#	X00(0.2)
20	30	HW	8/28/2012	REALTEK	Codec AGND to DGND modify	Replace C981, C982, C983 0.1uf by R5,R6,R15 0ohm	X00(0.2)
21	50	ESD	8/29/2012	COMPAL	Reserve GPU_HOT# control by H_PROCHOT#	Reserve H_PROCHOT# with level shift circuit to control GPU_HOT#	X00(0.2)

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Title		EE P.I.R (1/4)	
Size	Document Number	Rev	
	LA-9411P	1.0	
Date:	Wednesday, April 10, 2013	Sheet	72 of 77

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Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
22	24	ME	8/30/2012	COMPAL	ME request	Change SW1 power switch to SN11100580L SKRBAAE010_4P~D	X00 (0.2)
23	45	HW	9/3/2012	DELL	GPIO MAP2.4	1.Assign ECE5048_TX at 5048 GPIOE1/TXD 2.Remove 1.8V_RUN_PWRGD across X5 at 5048 GPIOK2 pin B10. 3.Move USB_PWR_SHR_EN# to GPIOK2 pin B10 4.Free up 5048 GPIOG3 (DYN_TURB_PWR_ALRT#),de-populate R796	X00 (0.2)
24	35	HW	9/4/2012	COMPAL	Follow INTEL Check list 1.0 reserve JAPS1 pin4, 7 connection	1.Reserve JAPS1 PIN4 of R23 SIO_SLP_S5# and R17 +3.3V_ALW_PCH 2.Reserve JAPS1 PIN7 of R24 +3.3V_ALW	X00 (0.2)
25	46	HW	9/18/2012	COMPAL	Added a 0ohm at U51 VTR_ADC pin.	Added R839 0ohm between +3.3V_ALW and U51.A58 pin.	X01 (0.3)
26	47	HW	9/19/2012	INTEL	Stuff RTC cell can't power on issue	Reserve R1636 pull down resistor on PCH_RSMRST#_Q.	X01 (0.3)
27	20,46	HW	9/24/2012	COMPAL	GPIO MAP2.5	1.Remove POA_WAKE# at 5075 VCI_INT3# pin B68 2.Remove FP_POA_EN at 5048 GPIOI7/PWM5 pin A44. 3.Rename LANWAKE# to EC_WAKE# at 5048 GPIOI5/PWM2 pin B1. 4.Add LANWAKE# connect to 5075 pin B27 5.Reserve 0ohm between LANWAKE# and EC_WAKE#	X01 (0.3)
28	11	HW	9/24/2012	COMPAL	HSW will internally power gate the VDDQ rail (+1.35V_CPU_VDDQ)	1.De-populated the +1.35V_CPU_VDDQ DC to DC circuit 2.add these two PJP5, PJP6 4x4mm Jumper between +1.35V_CPU_VDDQ and +1.35V_MEM power net.	X01 (0.3)
29	46	HW	9/24/2012	COMPAL	Follow CRB1.2 PECI circuit	De-populate PECI_EC_R C290 CAP.	X01 (0.3)
30	36	HW	9/24/2012	COMPAL	O2 Request	Add C802 0.1uF cap on SD_CD#.	X01 (0.3)
31	30	HW	10/03/2012	COMPAL	When no external power, it Sleeve will be floating mode and no reference GND.	Add AUD_NE_MUTE# to control Sleeve pin.	X01 (0.3)
32	16	HW	9/26/2012	COMPAL	Follow CRB, PCH_DPWROK circuit	Add RH120 100Kohm PD and close to PCH site.	X01 (0.3)
33	32	HW	9/26/2012	COMPAL	Follow EDS, Change USB30_SMI# (GPIO13) pull up power rail to +3.3V_ALW_PCH.	Change R514.1 to +3.3V_ALW_PCH	X01 (0.3)
34	38	HW	10/02/2012	Asmedia	Asmedia ASM1467 spec modify	1.Pin7 GND chage DE_A 2.Pin6 Reserved change to GND 3.Pin16 MOSEL change to Reserved 4.Pin17 DE_A change to MOSEL	X01 (0.3)
35	27	HW	9/26/2012	COMPAL	Change EDP to LVDS converter solution to RTD2136R	1.Change U27 P/N:SA000067100(S IC RTD2136R-CG QFN 48P DP/LVDS CTRL) 2.Remove R102,R103 0ohms 3.Remove R107 4.7Kohm 4.Add R108 4.7Kohm 5.Remove U26 CAT24C64WI-GT3_S08_EEROM	X01 (0.3)
36	28	HW	10/02/2012	COMPAL	Fix LCD T3 timing issue	Add R115 0ohm between LCD_ENVDD_CVT and U55.4 net to control +LCD_VDD power net.	X01 (0.3)
37	30	HW	10/04/2012	COMPAL	Reserve Support universal jack	1.C195,C196 4.7U_0603_6.3V6K~D 2.R198,R199 1K_0402_5% 3.R209,R210 4.7K_0402_5%~D 4.D11,D12 RB751VM-40TE-17_SOD323-2~D	X01 (0.3)
38	20,35	HW	10/05/2012	COMPAL	GPIO MAP2.6	1.Add SMART_DET# on PCH GPIOI5 and JUSH1 pin11. 2.Move EC_WAKE# from ECE5048[L]5 to MEC5075 GPIOI52. 3.Add ECE5048_PWRGD to MEC5075 GPIOI02 4.Add AND Gate of ECE5048_PWRGD, RUNPWROK to AND_PWRGD on ECE5048 A4 pin 5.Remove R842 pull up resistor	X01 (0.3)

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Compal Electronics, Inc.		
Title EE P.I.R (2/4)		
Size	Document Number LA-9411P	Rev 1.0
Date: Wednesday, April 10, 2013	Sheet 73	of 77

Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
39	30	HW	10/08/2012	COMPAL	Remove IDT& TI Audio codec co-lay circuit	Remove IDT& TI Audio codec co-lay circuit	X01 (0.3)
40	37	HW	10/08/2012	COMPAL	Remove +1.5V_RUN power rail on JMINI3 card	1.Remove +1.5V_RUN power rail on JMINI3 card of pin6, 28 and 48 2.Remove C619, C620 cap	X01 (0.3)
41	54	HW	10/11/2012	COMPAL	Correct DGPU_PWR_EN# behavior	Add QV5	X01 (0.3)
42	30	HW	10/11/2012	REALTEK	Follow Realtek recommend circuit	1.Change L91,92,93,94 to R41,42,43,44 0_0603_5%~D 2.Change C973,974,975,76 1000P_0402_50V8-J 3.Change R1680,1681,1682,1683 0_0402_5%~D	X01 (0.3)
43	11	HW	10/25/2012	COMPAL	Follow CRB1.5 design	1. De-populate 10UF CC26,CC27,CC28,CC29,CC30,CC31,CC32,CC33 2. De-populate 22UF CC41,CC37,CC42,CC43,CC38,CC44,CC39,CC45.CC46 3. De-populate 330UF CC34	X01 (0.3)
44	11	HW	10/25/2012	COMPAL	Support Deep SX mode	1. De-populate RH79 0_0402 2. Populate R802 0_0402	X01 (0.3)
45	30	HW	12/25/2012	COMPAL	Follow Realtek recommend circuit	1.Change R1658,R1095 to jump 2.Change R1119 ,R1120 to 100K 3.Change R1677 R1679 to 9.1 ohm 4.Remove R25	X02 (0.4)
46	50	HW	12/25/2012	COMPAL	Follow AMD recommend	Change GPU_HOT# pull high fomr 100K to 4.7K	X02 (0.4)
47	28	HW	12/25/2012	COMPAL	Samsnug PANEL issue	Add pull down R1139 100K	X02 (0.4)
48	20	HW	12/25/2012	COMPAL	TLS issue	Change RH229 fomr 200K to 1K	X02 (0.4)
49	46	HW	12/25/2012	COMPAL	Follow DELL recommend	add 0ohm to short RUNPWROK and AND_PWRGD	X02 (0.4)
50	36	HW	12/25/2012	COMPAL	Follow GPIO map rev 3.0C	SP_TPM_LPC_EN reserve PCH GPIO22 to control	X02 (0.4)
51	13,14	HW	12/25/2012	COMPAL	Follow CRB1.5 DDR RAM M1&M3 circuit	Reserve circuit to control 1.+SA_DIMM1_VREFDQ ,+SA_DIMM2_VREFDQ 2.+SM_VREF_DIMM 3.DDR3_DRAMRST#_R	X02 (0.4)
52	30	HW	12/25/2012	COMPAL	Follow ESD	Remove D83,D23,D8,D37,DE1&DE2	X02 (0.4)
53	36	HW	03/28/2013	COMPAL	Follow O2 recommend	add R493 on SD_CD#	A00 (1.0)

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Title				EE P.I.R (3/4)	
Size	Document Number			Rev	
	LA-9411P			1.0	
Date: Wednesday, April 10, 2013				Sheet 74 of 77	

Version Change List (P. I. R. List)

Page 1

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	66	+GPU_CORE	8/29	AMD	GPU_CORE merged with one of AMD Chip power rail - VDDCI	Delete VDDCI Power rail page	X00 (0.2)
2	60	+DC_IN	8/29	Compal	ESD Team change solution	Change PD1 PD2 Solution	X00 (0.2)
3	68	Charger for DSC	8/29	Compal	SMBus connection is wrong	Swap net CHARGER_SMBDAT and CHARGER_SMBCLK	X00 (0.2)
4	67	+VGA_PCIE/ +1.8V_RUN_GFX	8/29	Compal	DGPU_PWR_EN signal pull high voltage net is wrong	Change PR692 Pin1 net from +3.3V_ALW to +3.3V_RUN	X00 (0.2)
5	61	3VALWP/5VALWP	8/29	Compal	Find tune 3V/5V OCP setting	Change PR105 from 110k to 115k for 3.3V Change PR106 from 82.5k to 86.6k for 5V	X00 (0.2)
6	62	1.35V/0.675VSP	8/29	Compal	Change Enable signal from SIO_SLP_S4# to SUS_ON by HW request	Pop PR210 and depop PR206	X00 (0.2)
7	63	1.05VSP	8/29	Compal	Fint tune 1.05VSP OCP setting	Change PR302 from 64.9k to 68.1k	X00 (0.2)
8	65	VCORE_ISL95812 for QC	8/29	Compal	Fint tune DC loadline	Change PR537 from 2.55k to 2.37k	X00 (0.2)
9	66	+GPU_CORE	8/29	AMD	Adjust OCP setting for +GPU_CORE merge with VDDCI	Change PR659 from 787 to 1.37k	X00 (0.2)
10	66	+GPU_CORE	8/29	AMD	Adjust initial voltage from 1.125V to 0.85V	Pop PR602 PR604 PR608 PR605 PR610 PR612 Depop PR606 PR611 PR613 PR601 PR603 PR609	X00 (0.2)
11	65	VCORE_ISL95812 for QC	9/25	Compal	Fint tune DC loadline	Change PR535 from 475ohm to 511ohm Change PR537 from 2.37k to 2.55k	X01 (0.3)
12	65	VCORE_ISL95812 for QC	9/25	INTERSIL	Change schematic setting for new version IC (Rev3p0)	Change PR529 from 0 to 6.04k Change PR512 from 21k to 16.9k Change PR507 from 49.9k to 21k Change PR509 from 34k to 3.24k	X01 (0.3)
13	65	VCORE_ISL95812 for QC	9/25	Compal	Fint tune IMON	Change PR521 from 90.9k to 100k	X01 (0.3)
14	68	Charger for DSC	9/28	TI	Schematic setting for charger IC	Change PR722 from 0 to 4.02k	X01 (0.3)
15	69	Selector	9/28	Compal	Can not power on with only slice battery	Add PD819 and DOCK_SMB_ALERT# control signal	X01 (0.3)
16	69	Selector	9/28	Compal	Turn on DOCK_PWR_BAR NVDC blocking MOSFET(PQ815) to charge and discharge slice battery	Add PR882 and SLICE_BAT_PRES# control signal to replace SLICE_PREF_EN EC signal	X01 (0.3)
17	69	Selector	9/28	Compal	Turn off DOCK_PWR_BAR NVDC blocking MOSFET(PQ815) when AC connect to other NB or DOCK	Add PR886 PR887 and DOCK_DET# control signal to replace SLICE_PREF_EN EC signal	X01 (0.3)
18	60	+DC_IN	10/8	Compal	Reserve circuit for droop module battery function	Reserve PQ7 PD7 PR26 PC17 location	X01 (0.3)
19	69	Selector	10/8	Compal	Reserve circuit for droop module battery function	Reserve PR888 PR890 PR892 location	X01 (0.3)

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Compal Electronics, Inc.		
Title		
PWR_PIR 1		
Size	Document Number	Rev
	LA-9411P	0.4
Date:	Wednesday, April 10, 2013	Sheet 75 of 77

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Version Change List (P. I. R. List)

Page 2

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
20	69	Selector	10/8	Compal	Abnormal waveform in PBAT_PRES# when remove battery	Change PD811 and PD804 location	X01 (0.3)
21	69	Selector	10/8	Compal	Avoid voltage appearing at the docking connector when either slice battery or E-Dock is not connected to notebook	Add PQ826	X01 (0.3)
22	65	VCORE_ISL95812 for QC	10/8	Compal	Remove the 1.05V_0.8V_PWROK connection by HW request	Delete PR517	X01 (0.3)
23	63	1.05VSP	10/8	Compal	Remove the 1.5V_RUN_PWRGD connection by HW request	Delete net 1.5V_RUN_PWRGD	X01 (0.3)
24	68	Charger for DSC	10/11	Compal	Reserve circuit for system throttling switching from AC to DC if droop module battery function	Reserve PU704 PC733 PR748 PQ710 PQ708 location	X01 (0.3)
25	60	+DC_IN	11/20	Dell	Reserve module battery connector circuit for droop module battery function	De-pop MBATT1 PC2 PR4 PR3 PR5 PL1 PR2 PD1 PC1 PJP1	X02 (0.4)
26	60	+DC_IN	11/20	Dell	Add Main battery control signal circuit for droop module battery function	Pop PQ7 (DMG2301U-7) PD7 (SDMK0340L-7-F) PC17 (1500pF) PR26 (0 ohm)	X02 (0.4)
27	60	+DC_IN	11/20	Compal	Reserve +PWR_SRC to +PWR_SRC_S Circuit by HW request	De-pop PQ3 PQ5 PR21 PC15 PR24 PR19 PR17 PC6 PC7	X02 (0.4)
28	60	+DC_IN	11/20	Compal	Change EMI solution by EMI request	Delete PL6 PD6 and add PJP4	X02 (0.4)
29	68	Charger for DSC	11/20	Dell	Add circuit for CPU freq to LFM mode when heavy loading plug out AC, because this function is built in module battery function controller IC - CD3302, droop module battery will not use CD3302 controller.	Pop PU704 (74AHC1G08GW) PC733 (0.1uF) PQ710 (DMN65D8LW-7) PR748 (100K)	X02 (0.4)
30	68	Charger for DSC	11/20	Compal	Use one dual N package part to replace two NPN Mosfet	Change PQ707 PQ708 from DMN65D8LW-7 to DMN66D0LDW-7 (PQ707A PQ707B)	X02 (0.4)
31	69	Selector	11/20	Dell	Reserve module battery circuit about trigger PROCHOT# when active battery is removed from system.	De-pop PU802 PC802 PU803 PC804 Pop PR888 (0 ohm)	X02 (0.4)
32	69	Selector	11/20	Dell	Reserve controller - CD3302 solution for droop module battery circuit	De-pop PU808 PR834 PR837 PR842 PR848 PR851 PR853 PR856 PC814 PR861 PR865 PR867 PR871 PR873 PR876 PR836 PR841 PR845 PR852 PQ910 PR880 PR878 PR879	X02 (0.4)
33	69	Selector	11/20	Dell	Reserve module battery charging and discharging path circuit	De-pop PQ808 PD803 PR800 PR803 PR805 PD804 PD805 PQ803 PD801 PQ804 PR809 PC800 PR806 PD802 PD809	X02 (0.4)
34	69	Selector	11/20	Dell	Change battery control signal for droop module battery function	De-pop PD812 PR889 PR891 Pop PR890 (0 ohm) PR892 (0 ohm)	X02 (0.4)
35	69	Selector	11/20	Compal	Change Main source for EOL issue.	Change PQ801 PQ814 PQ822 PQ823 from FDN338P_G to NTR4502PT1G	X02 (0.4)

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Compal Electronics, Inc.		
Title		
PWR_PIR 2		
Size	Document Number	Rev
	LA-9411P	0.4
Date: Wednesday, April 10, 2013		
Sheet 76 of 77		

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
36	69	Selector	11/20	Compal	Use one dual diode package part to replace two discrete diode part	Change PD810 PD814 PD813 PD816 PD815 PD817 from SDMK0340L-7-F to BAT54CW (PD814 PD816 PD817)	X02 (0.4)
37	70	PROCESSOR DECOUPLING	11/20	Compal	Move GPU Core output MLCC cap to power side by HW request	Change CV172 CV174 CV175 CV183 location to PCV172 PCV174 PCV175 PCV183	X02 (0.4)
38	68	Charger for DSC	11/20	Compal	Change bootstrap resistor size	Change PR715 size from 0402 to 0603	X02 (0.4)
39	69	Selector	11/20	Compal	Use one package part to replace dual n package part	Change PQ802 from DMN66D0LDW-7 to DMN65D8LW-7	X02 (0.4)
40	65	VCORE_ISL95812 for QC	12/25	Compal	VCCIO_OUT 6KHz noise issue. Request by H.W.	Add PC548 (1uF)	X02 (0.4)
41	65	VCORE_ISL95812 for QC	12/25	INTERSIL	Fine tune Iout accuracy	Change PR535 from 511 Ohm to 470 Ohm. Change PR521 from 100kOhm to 100kOhm. Change PC500 from 0.01uF to 1000pF. Change PC539,PC540,PC544 from 0.22uF to 0.022uF. Change PR510,PR538,PR553 from 10kOhm to 100kOhm. Add PR558 (4.3M Ohm)	X02 (0.4)
42	68	Charger for DSC	12/25	TI	For Input current sense stabilize	Change PC703 from 0.1uF to 1uF	X02 (0.4)
43	68	Charger for DSC	12/25	TI	Change cell pin pull high reference voltage from +3.3V_ALW to BQ24715_REGN	Depop PR720 and pop PR746	X02 (0.4)
44	60	+DC_IN	12/25	Compal	GPIO net - AC_DIS# is high active. Corrent net name.	Change PQ6A pin.5 net name from AC_DIS# to AC_DIS.	X02 (0.4)
45	69	Selector	12/25	Compal	GPIO net - AC_DIS# is high active. Corrent net name.	Change PR828 pin1 net name from AC_DIS# to AC_DIS.	X02 (0.4)
46	68	Charger for DSC	1/7	Compal	Reserve input cap location for input voltage overshoot issue. This issue fix in PG1.3	Reserve PC734 PC735	X02 (0.4)
47	68	Charger for DSC	1/7	Compal	IAC peaks with VCORE EMI bead (PL504). reaches 8 A, triggers PROCHOT	Reserve PC736 PC737 PC738	X02 (0.4)
48	68	Charger for DSC	1/7	DELL	AC+ E5 Battery will not active H_PROCHOT funtion	Add PR749 and EC signal	X02 (0.4)
49	60	+DC_IN	2/6	Compal	Change PD2 material by ESD team request.	Change PD2 material and add PD4.	X02 (0.5)
50	69	Selector	2/6	Compal	To avoid +DOCK_PWR_BAR leakage voltage when system only with main battery	Add PD821 PQ820 PR896 PR897 PQ830 PC818 PU809	X02 (0.5)

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Compal Electronics, Inc.		
Title		
PWR_PIR 3		
Size	Document Number	Rev
	LA-9411P	0.4
Date: Wednesday, April 10, 2013		
Sheet 77 of 77		